SIGE HBT BICMOS RF FRONT-ENDS FOR RADAR SYSTEMS

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SIGE HBT BICMOS RF FRONT-ENDS FOR RADAR SYSTEMS

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To my family, friends, and loved ones

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SUMMARY

The objective of this research is to explore the possibilities of developing transmit/receive (T/R) modules using silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) BiCMOS technology to integrate with organic liquid crystal polymer (LCP) packages for the next-generation phased-array radar system. The T/R module requirements are low power, compact, lightweight, low cost, high performance, and high reliability. All these requirements have provided a very strong motivation for developing fully monolithic T/R modules. SiGe HBT BiCMOS technology is an excellent candidate to integrate all the RF circuit blocks on the T/R module into a single die and thus, reducing the overall cost and size of the phase-array radar system. In addition, this research also investigates the effects and the modeling issues of LCP package on the SiGe circuits at X-band. The contributions from this research work are summarized as follows:

1. Design of an X-band SiGe power amplifier (PA) for monolithically integrated phased-array T/R modules.
2. Design of a low-loss and low-noise tunable, monolithic X-band SiGe active bandpass filter [1].
3. Investigation of temperature effects on SiGe tunable filter [1].
4. The extraction of a lumped-element, equivalent circuit model for via interconnections in 3-D packages using a single via structure with embedded capacitor [2].

5. De-embedding transmission lines using a full-wave EM-simulated pad model [3].
6. Design of a low-power and low-voltage X-band SiGe HBT low-noise amplifier (LNA) [4].
7. Design of an X-band to Ka-band single-pole double-throw (SPDT) switch [5].
8. Investigation of packaging effects of multiple X-band SiGe LNAs embedded in an organic LCP substrate [6].
9. Design of a novel Modified Wilkinson power combiner [6].

CHAPTER I

INTRODUCTION

1.1 Radar System

Radar, *radio detection and ranging,* was developed and deployed during the Second World War [7]. During the Second World War, it was believed that whichever side spotted an enemy plane or ship first would have a higher chance of winning the battle [8]. The Allies began to develop a technology to assist them in the battle for detecting distant objects that are hundreds of miles away and even in the dark. The US Navy came out with the acronym for this technology, known as RADAR. With the advancement in technology, radar systems are also used for commercial applications such as weather monitor, remote sensing, and collision avoidance.

Figure 1 shows the basic working principle of a radar system. The transmitter produces an electromagnetic (EM) wave that consists of short and strong signal radio frequency (RF) pulses. When the EM wave hits the target, it is reflected back to the receiver. Based on the received EM wave, the radar system is able to compute the velocity, distance, and position of the target.

1.2 Radar System Evolution

The types of antennas use in a radar system will determine the radar performance. Before 1960s, most antennas were rotating dish type. In a rotating dish antenna, mechanical parts are used to steer the beams. The main disadvantage of using a mechanical steering is that its scanning rate is usually limited and slow. For military applications such as the missile warning system and space surveillance, the radar scanning rate has to be fast.

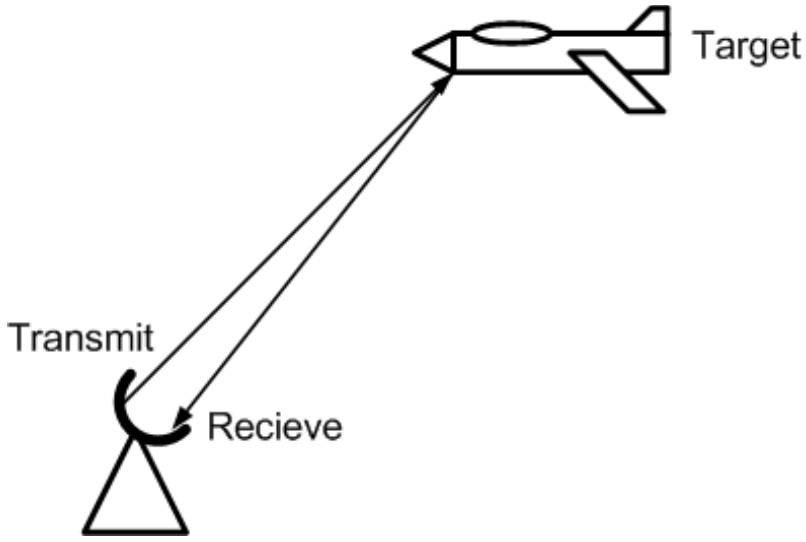


Figure 1: Basic principle of a radar system

As a result, beam steering antennas are preferred. In a beam steering antenna, the beams are formed by controlling the signal phase propagated from each antenna element to provide a constructive / destructive interference, so that the beams can be steered in a desired direction. The phase can be easily controlled electronically, allowing the beam to be steered very quickly without having to move the antenna. Thus, the beam steering antennas have significant higher scanning rate and this leads to the development of phased-array radar systems. Figure 2 shows the evolution of radar systems.

1.3 Phased-Array Radar: Passive Vs. Active

The phased-array radar systems consist of two main groups: the passive and the active. Figure 3 shows the schematics of both the passive and the active phased-array radar systems. One of the main differences is that the passive phased-array radar system has a centralized T/R architecture, while the active phase-array radar system has multiple T/R architectures.

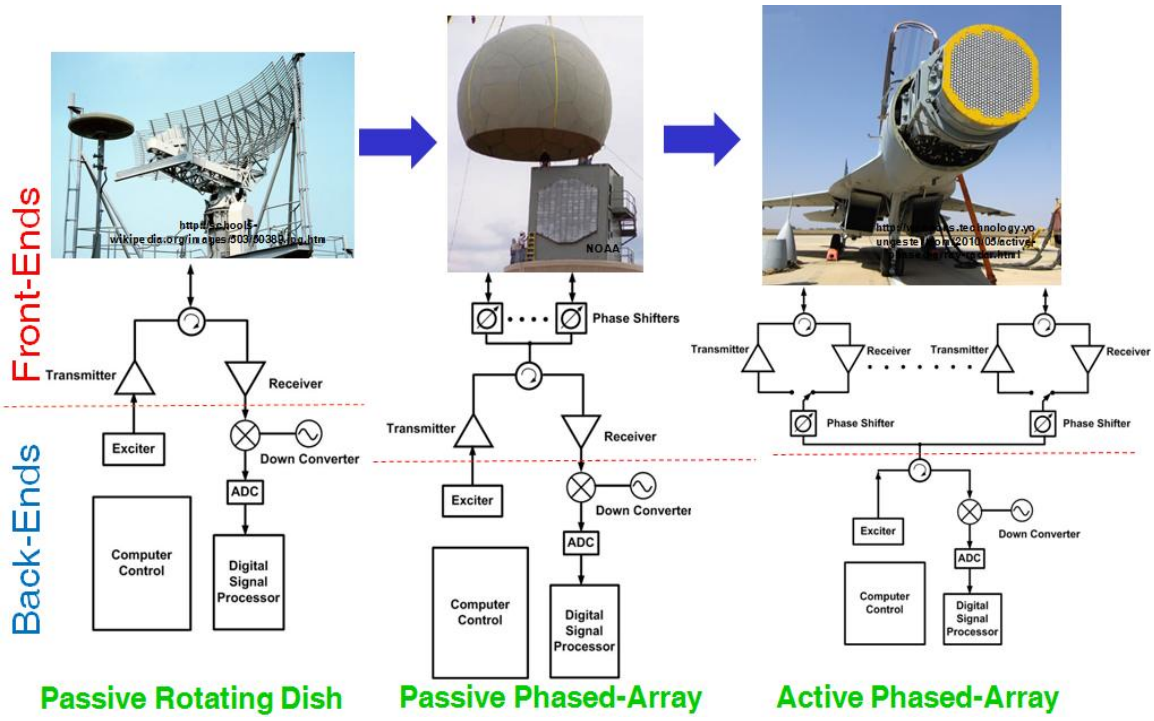


Figure 2: Evolution of radar systems

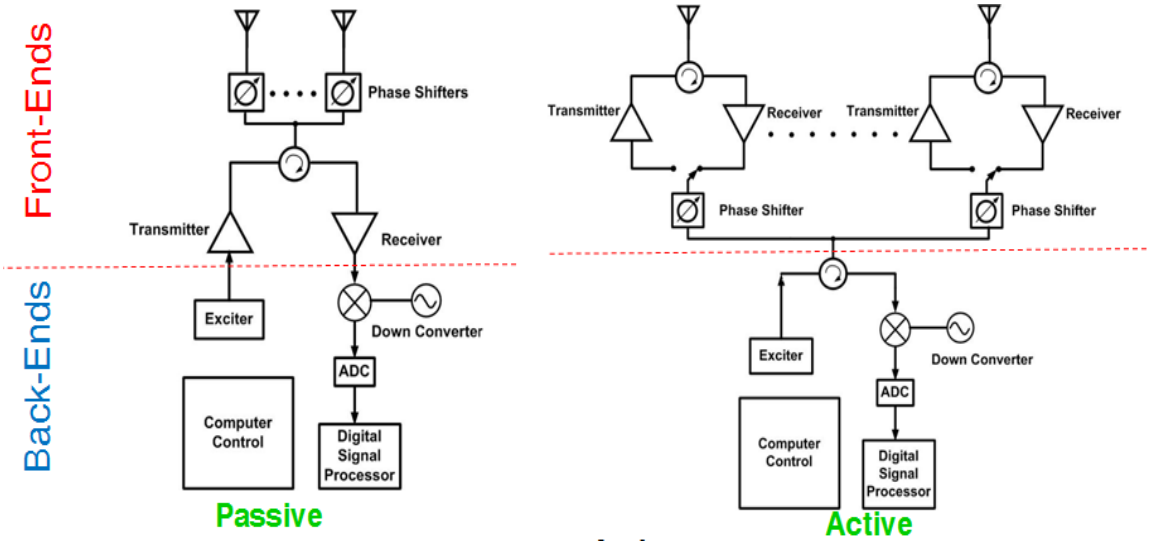


Figure 3: Phased-array radar system: passive and active.

Table 1 compares the pros and cons between the passive and the active phased-array radar systems. In Table 1, it is shown that the active phased-array radar system

tends to have better performance and reliability than the passive phased-array radar system. In addition, the requirements for the LNAs and PAs in the active phased-array radar system are usually less stringent, making the overall system design more realizable. Although the cost of the passive phased-array radar system is lower, it is believed that the cost of the active phased-array radar system will potentially reduce with time.

1.4 Active Phased-Array Radar T/R Modules

In a communication system, the RF front-end is generally a group of circuit blocks between the antenna and the digital baseband. An active phased-array radar system usually has multiple transmit/receive (T/R) modules at its RF front-end [9] . The T/R modules vary the amplitude and phase of a signal feeding each antenna element, so that the effective radiation pattern of the array can be reinforced in a desired direction, as shown in Figure 4 [10].

A typical T/R module for a phased-array radar system consists of a circulator, a low-noise amplifier (LNA), a power amplifier (PA), and a phase shifter. To reduce the physical size of T/R modules, the phase shifter is usually shared by the transmitter and the receiver using a single-pole double-throw (SPDT) switch. The performance and the cost of the phased-array radar system are mainly dominated by the T/R modules.

Table 1: Comparison between the passive and the active phased-array radar systems.

	Passive	**Active**
Architecture	Centralized T/R	Multiple T/Rs
Insertion Loss	Higher	Lower
Noise Figure	Higher	Lower
Reliability	Low	High
Design Specification	Difficult to meet	Easier to meet
Cost	$	$$ (Potential cost reduction with time)

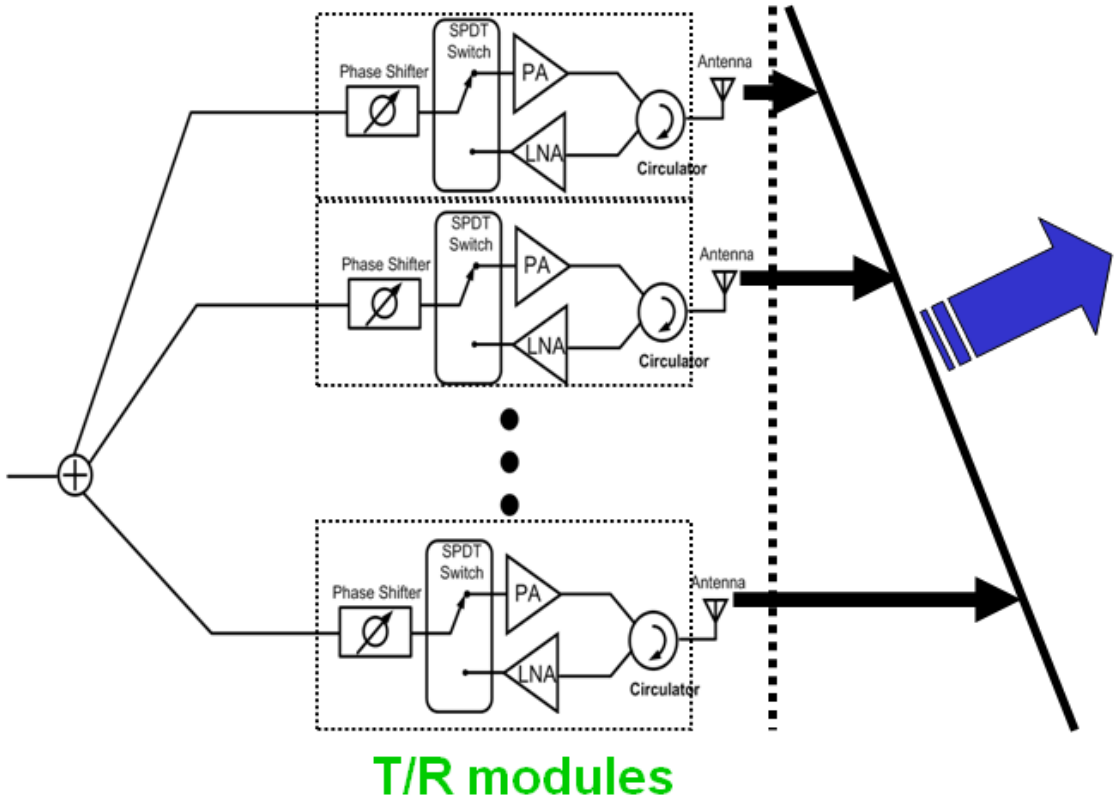


Figure 4: Transmit/receive (T/R) modules in an active phased-array radar system [9].

The performance of a radar system is evaluated based on the figure-of-merit (FOM), which is defined as

$$FOM = PAG\,, \tag{1}$$

where P, A, and G are the average transmitter power, the aperture area, and the antenna gain, respectively [11].

From (1), the FOM terms for a phased-array radar system are given as

$$P = P_e N\,, \tag{2}$$

$$A = A_e N\,, \tag{3}$$

and

$$G = G_e N \approx \frac{4\pi A_e}{\lambda^2} N\,, \tag{4}$$

where P_e, A_e, and G_e are the average transmitter power, the aperture area, and the gain of a single antenna element in the phased array, respectively, λ is the operation wavelength, and N is the number of antenna elements in the array [12]. Combining (1) through (4), the FOM of the phased-array radar system can be further expressed as

$$FOM = P_e A_e^2 \frac{4\pi}{\lambda^2} N^3. \quad (5)$$

In many situations for a fixed FOM, P_e can be drastically reduced by increasing N, which prevents the radar system from overheating [13].

The current phased-array radar T/R modules are typically multi-chip modules (MCMs) containing the III-V monolithic microwave integrated circuits (MMICs). As a result, an increase in N would also increase the cost of the radar system because of the expensive III-V MMICs. The cost of each MCM could be as high as 1,000 dollars [14]. Therefore for the T/R modules, there is a strong motivation to replace the III-V technologies with a much lower cost silicon-based technology. Figure 5 shows an X-band T/R module developed by EADS. The size of the T/R module is 64.5 x 13.5 mm^2. The T/R module contains a PA, a ferrite circulator, a monolithically integrated limiter, and a low-noise pre-amplifier. The T/R module is implemented using gallium arsenide (GaAs) technology.

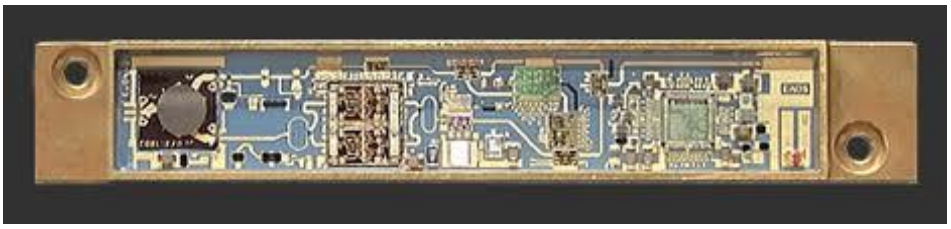


Figure 5: GaAs T/R module (courtesy of EADS).

1.5 MMIC Packaging Considerations

Understanding the electrical characteristics of a high-frequency package and its interconnects is important to optimize the circuit performance. At high frequency (> 3 GHz), the parasitics arising from the package interconnects are no longer transparent to electrical performance and need to be explicitly taken into consideration during the design stage. One way to model the parasitics is by performing a full-wave EM simulation. However, the EM simulations tend to be time consuming and complicated, especially for circuits with many package interconnects. It is highly desirable to implement equivalent circuit models for the package interconnects to be used in the circuit simulations to bypass the need for the EM simulations.

In a packaged MMIC, wirebonding is the primary method of making interconnects between the MMIC and the package. The wirebond interconnect is convenient and easy to implement [15], but it has the tendency to introduce high loss and mismatch especially at higher frequencies because of large parasitic inductance and resistance [16]. Figure 6 shows the S_{11} simulations of a 1 mil diameter bondwire that is terminated with 50 Ω load, from 1 to 40 GHz. The wire length is ranged from 10 to 40 mil.

The S_{11} simulations demonstrate that the wire tends to be more inductive as the wire length increases. The impedance of the wire is expressed as

$$\text{impedance} = 2\pi fL, \tag{6}$$

where f is the operating frequency and L is the inductance of the wire. From (6), it is shown that the impedance of the wire increases with frequency. Therefore, the wire length is going to have more impact on the impedance matching between the MMIC and the package at higher frequencies.

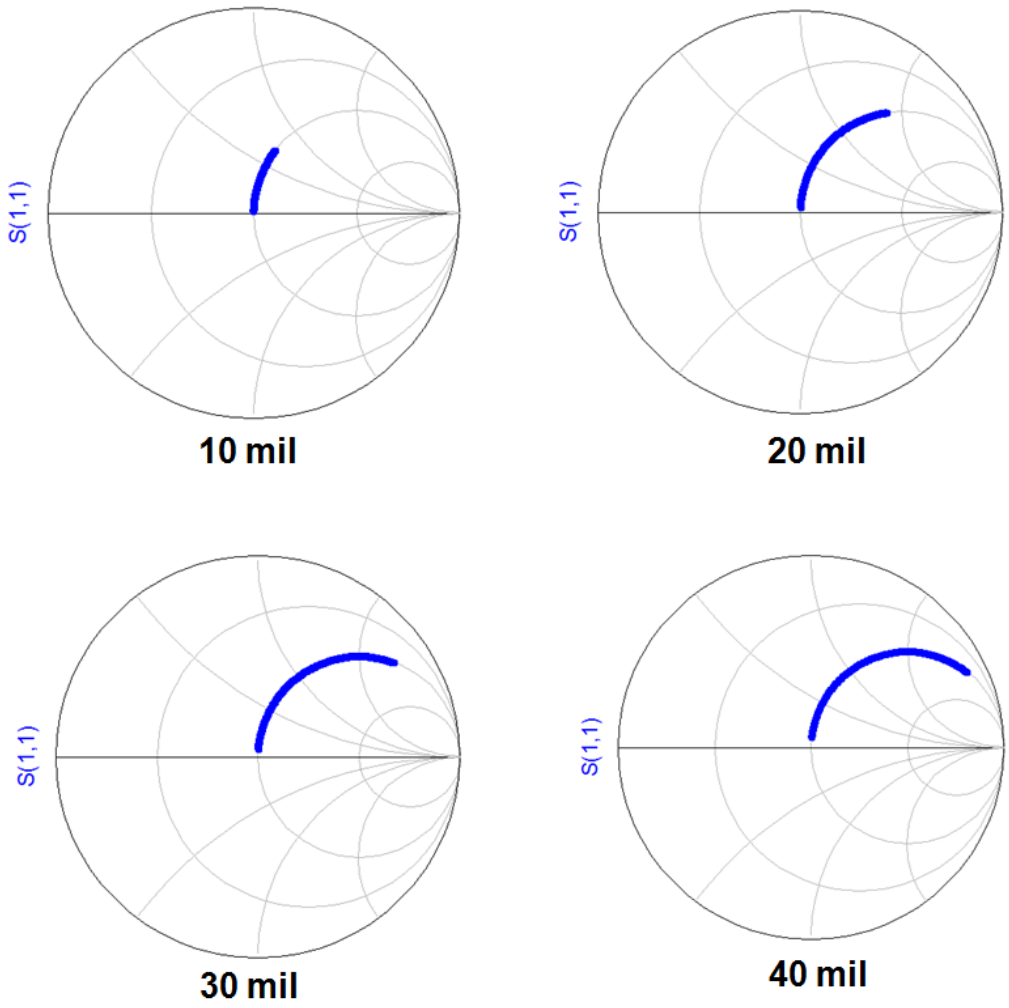


Figure 6: S_{11} simulations of 1 mil diameter bondwire for different wire lengths.

As a result, there is a strong interest to explore the possibilities of embedding multiple MMICs in multi-layer liquid crystal polymer (LCP) substrates for T/R modules [17] . The LCP is an organic material and offers a unique combination of properties. Recently, the LCP has gained much consideration as a potential high-performance microwave substrate as well as a RF packaging material. Besides being a low-cost dielectric material, the LCP has a low dissipation factor and a low water absorption

coefficient, making it a first choice material for developing multilayer antenna array. In addition, its coefficient of thermal expansion (CTE) can be adjusted through thermal treatments, facilitating integration of circuits in system-on-package (SOP) modules [18]. Using LCP antennas will also lead to weight reduction in radar systems. For airborne radar systems, the lightweight property of LCP enables the radars to mount onto smaller aircrafts, which helps to reduce the operating cost.

1.6 SiGe HBT BiCMOS Technology

In the past decade, the silicon germanium (SiGe) heterojunction bipolar transistor (HBT) bipolar-complementary metal-oxide semiconductor (BiCMOS) process has become a leading technology and is increasingly deployed in a wide variety of RF circuit applications. SiGe HBT BiCMOS integrated circuits (ICs) can be found in many communication devices such as the cellular handsets, wireless local area networks (WLAN) building blocks, global position system (GPS) systems, and radar systems. Figure 7 shows the application frequency bands for SiGe HBT BiCMOS technology [19].

The presence of Si-SiGe heterojunctions in the emitter-base (EB) and collector-base (CB) junctions causes the device physics of the SiGe HBT to be different from that of a conventional Si BJT [20]. The cross-section of SiGe HBT is shown in Figure 8.

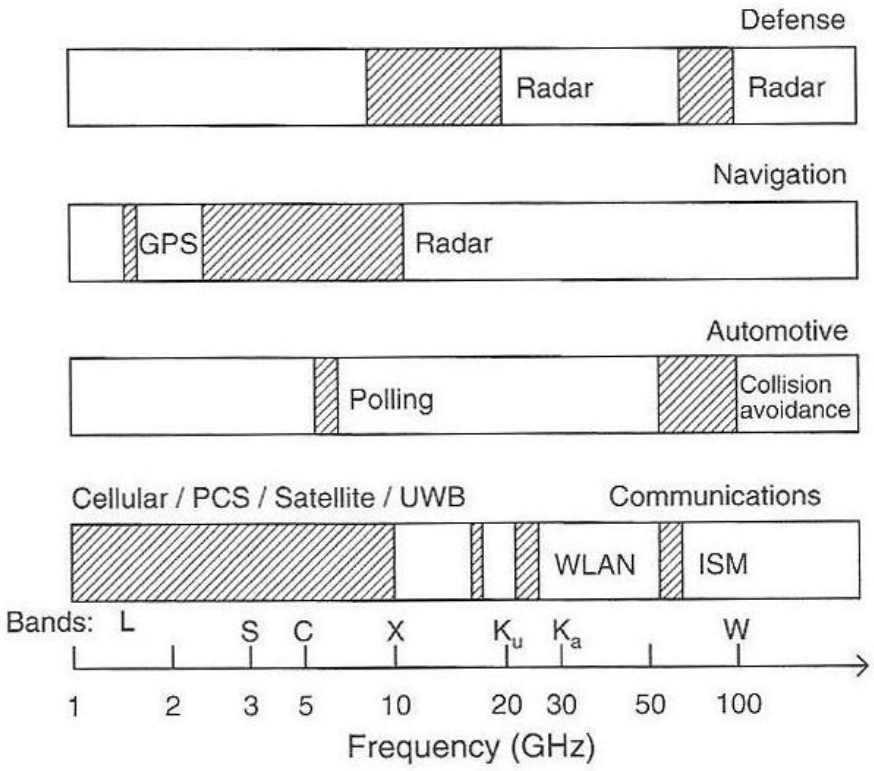


Figure 7: Application frequency bands for SiGe HBT BiCMOS technology [19].

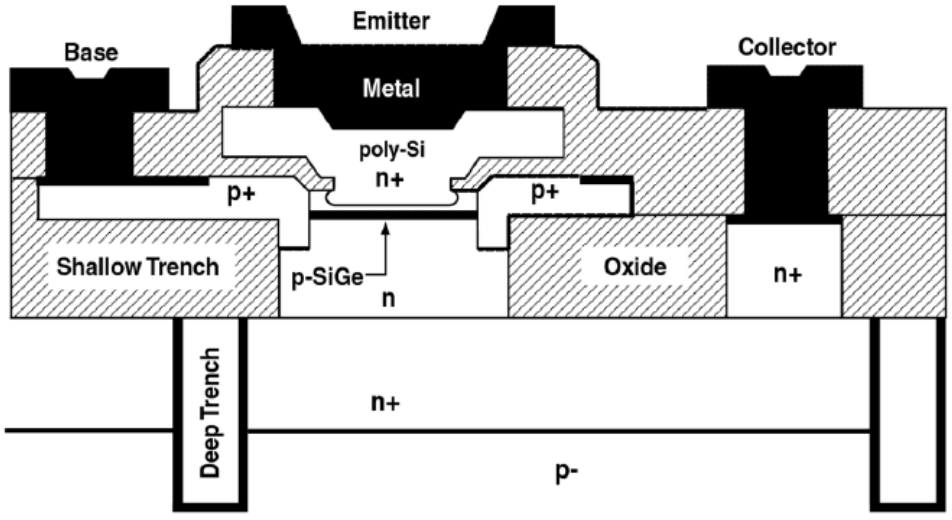


Figure 8: Cross-section of SiGe HBT [20].

SiGe HBTs utilize bandgap engineering to dramatically improve conventional silicon (Si) bipolar-junction transistor (BJT) performance. Figure 9 shows the energy band diagram for Si BJT and SiGe HBT, both biased in forward active mode at low-injection. As shown in Figure 9, when Ge is introduced into the base region, the potential barrier to injection of electrons from emitter into the base decreases, and this leads to more electron injection and higher current gain for the same base-emitter voltage (V_{be}). In addition, the presence of Ge in CB junction leads to a higher Early voltage.

The power consumption of each circuit block in the RF front-ends is a crucial design consideration, and often enough the power consumption has a direct impact on the operation cost. As shown in Figure 10, for a fixed collector current, SiGe HBT has a higher f_T than conventional Si BJT [21]. Thus in comparison, a SiGe HBT amplifier will have a higher gain and a lower power consumption than a Si BJT amplifier.

In a SiGe HBT BiCMOS technology, the SiGe HBT process maintains a strict compatibility with conventional CMOS manufacturing [22]. The ability of fabricating both SiGe HBT and CMOS technologies on a single wafer, has created many opportunities for mixed-signal ICs. The SiGe HBT technology offers a high speed and gain performance, which is desirable for many RF and analog applications. The CMOS technology offers high-input resistances, making it very suitable for constructing low-power logic gates in digital circuits.

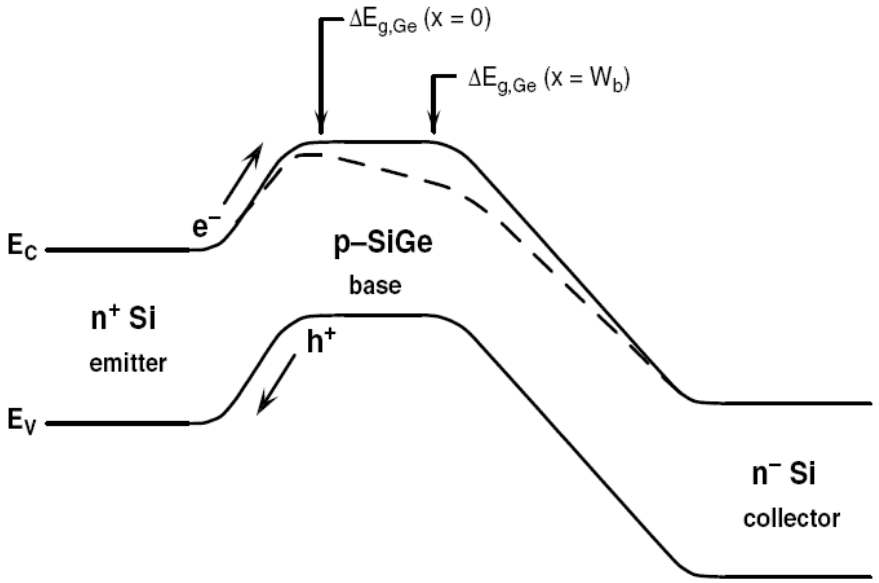


Figure 9: Energy band diagram for SiGe HBT (dashed) and Si BJT (solid) biased in forward active region [20].

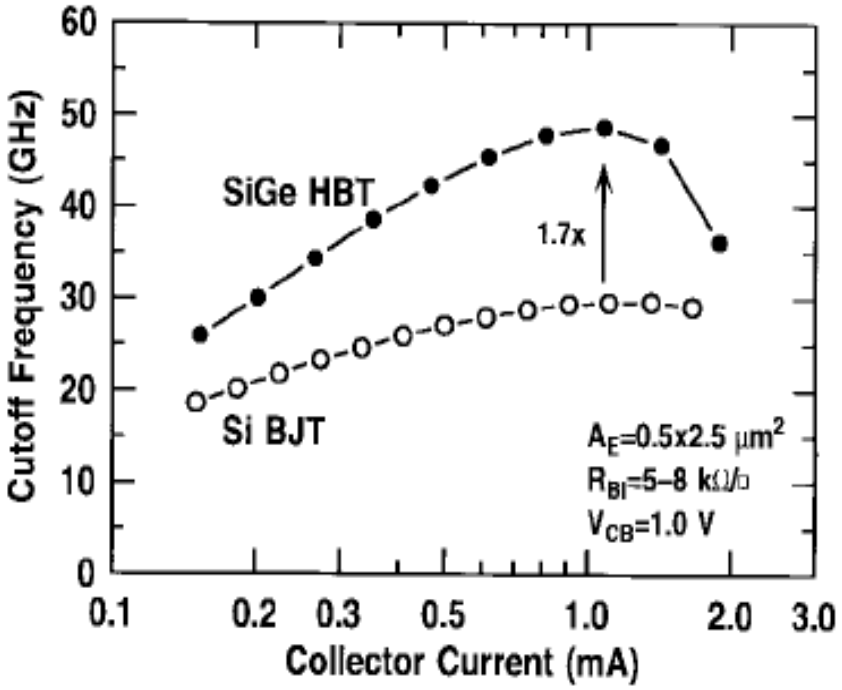


Figure 10: Comparison of the f_T as a function of collector current for a SiGe HBT and a Si BJT of comparable doping profile [21].

SiGe HBT is distinguished between different technology generations according to their *ac* performances, such as unity-gain-cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) [20], is shown as follows:

1. First generation – SiGe HBT with peak f_T in the range of 50 GHz
2. Second generation – SiGe HBT with peak f_T in the range of 100 GHz
3. Third generation – SiGe HBT with peak f_T in the range of 200 GHz
4. Fourth generation – SiGe HBT with peak f_T in the range of 300 GHz

As shown in Figure 11, the f_{max} and f_T of SiGe HBT has increased dramatically with each succeeding generation.

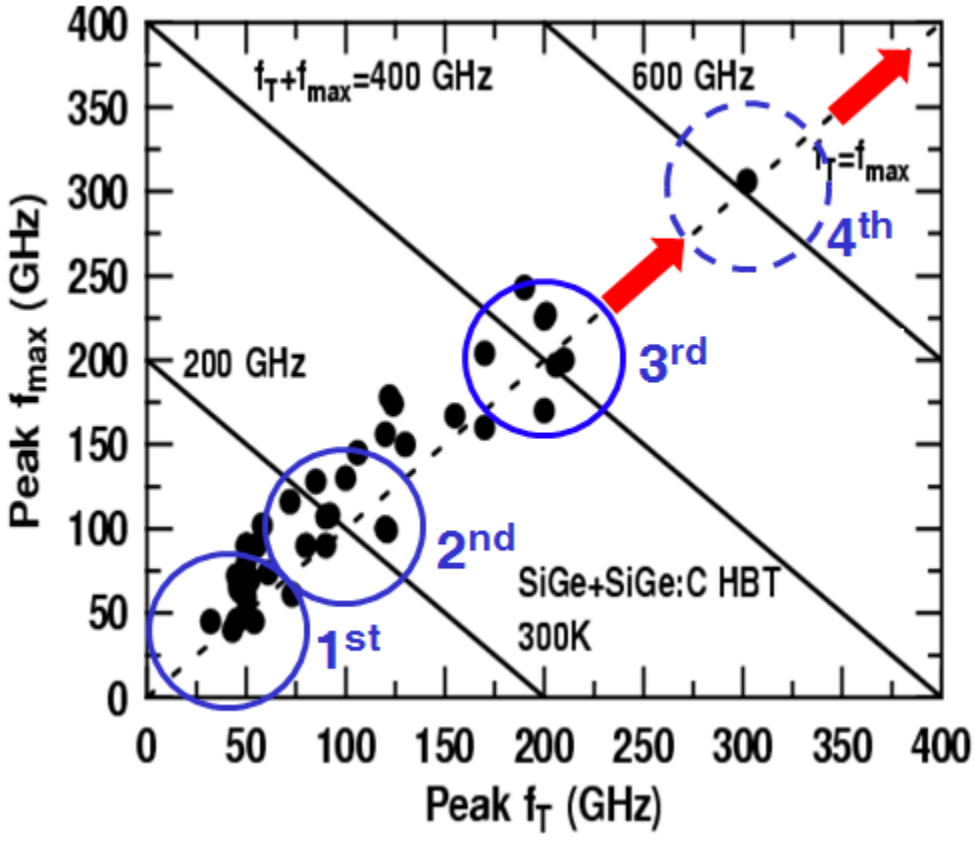


Figure 11: Measured f_{max} and f_T for a variety of generations of SiGe HBT BiCMOS technology [20].

III-V technologies have always been the main technology platform for monolithic microwave integrated circuits (MMIC) because of their high electron mobility and electron velocity, which enable the transistors to operate at high frequencies. However, unlike the SiGe HBT BiCMOS technology, it is difficult to integrate a III-V device with CMOS on a single wafer, since there is no decent grown oxide for III-V process. Thus, the applications of III-V technologies are limited as they do not offer a complete system-on-a-chip (SOC) solution. Over the years, the f_{max} and f_T of SiGe have increased and now more MMICs are fabricated using Si technology. Given the same wafer size, the cost of the SiGe HBT BiCMOS process is much lower than the III-V process, which leads to less expensive integrated circuits.

Since cost is an important factor to consider in system designs, more MMICs are designed based on CMOS process. However, for noise performance, the SiGe HBT technology definitely has a huge advantage over the CMOS technology. For instance, the $1/f$ noise and the thermal noise of CMOS are significantly higher than SiGe HBT. In order to compensate for the noise degradation in CMOS technology, very large devices and large operating current are usually required. Thus, given the same RF performance, SiGe HBT consumes much less power and is smaller in size, which is desirable for many modern communication systems. As shown in Figure 12, given the same device size, SiGe HBT BiCMOS technology has achieved a f_T higher (2.2 x) than CMOS technology, and given the same f_T performance, the cost of SiGe HBT BiCMOS technology is lower (0.5 x) than CMOS technology [23]. Considering all these factors, SiGe HBT BiCMOS technology offers the best trade-off in term of cost and performance.

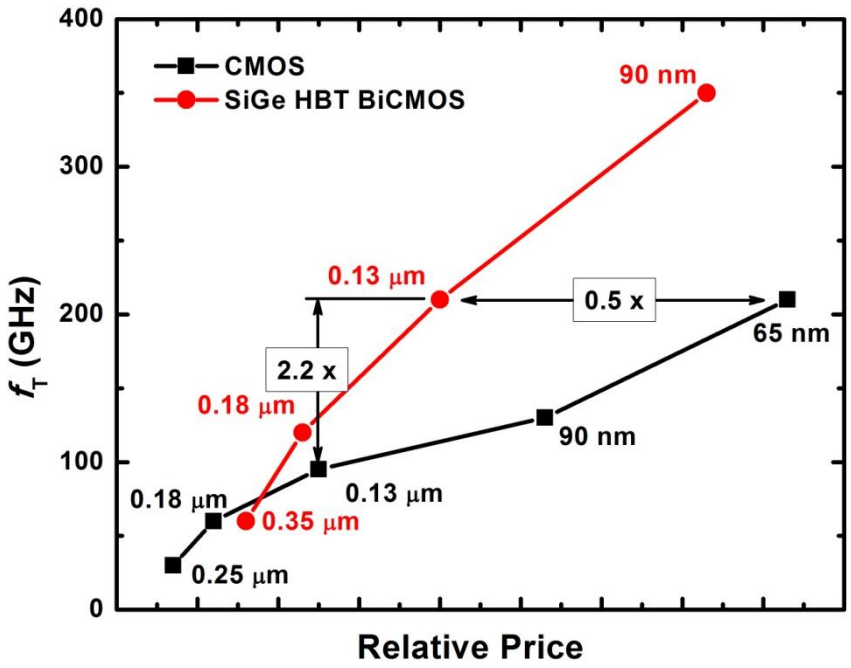


Figure 12: Price-performance comparison between SiGe HBT BiCMOS and CMOS technologies [23].

1.7 Motivation

The objective of the dissertation is to explore the possibilities of developing T/R modules using SiGe HBT BiCMOS technology to integrate with LCP package for the next-generation phased-array radar system. The T/R module requirements are low power, compact, lightweight, low cost, high performance, and high reliability. All these requirements have provided a very strong motivation for developing fully monolithic T/R modules packaging in the LCP substrate, thus achieving superior performance in the T/R modules.

1.8 Organization and Contributions of the Dissertation

The dissertation contributes to the designs of RF front-ends in radar systems and discusses issues of RF packaging for SiGe MMICs in T/R modules.

Chapter II presents the design of an X-band SiGe power amplifier (PA) for monolithically integrated phased-array T/R modules. The SiGe PA was implemented in a 130 nm SiGe BiCMOS technology and the total die area including the bond pads is 0.59 x 0.94 mm^2. At 9.5 GHz, the X-band PA has a gain of 15.4 dB, output-referred 1-dB compression point (P_{1dB}) is 16 dBm, output saturation power (P_{sat}) is 19 dBm, and maximum power-added efficiency (PAE) is 18.5%.

Chapter III (also submitted for reviews in [1]) presents a low-loss and low-noise tunable, monolithic X-band active bandpass filter (BPF) implemented in 130 nm SiGe BiCMOS process technology (IBM 8HP). The filter occupies 1.85 x 0.70 mm^2 (including bondpads) and consumes a *dc* power of 2.75 mW. When the tuning voltage is set between 0 and 2 V, the tunable SiGe BPF has a tunable center frequency (f_c) of 8.3 to 11.7 GHz, has an insertion loss less than 1.2 dB, and a 3-dB bandwidth between 2.2 and 3.0 GHz (a fractional bandwidth of 26.5%). The worst-case measured IIP_3 and input P_{1dB} are -7.1 dBm and -13.5 dBm, respectively at 8.3 GHz. The measured noise figure of the filter is 3.66 dB. The filter S-parameters were measured across temperatures ranging from 90 to 398K. At cryogenic temperature (90 K), the filter bandpass gain shows an improvement of more than 1 dB. At high temperature (398 K), the degradation in the bandpass gain is less than 2.7 dB.

Chapter IV (also published in [2]) presents the extraction of a lumped element, equivalent circuit model for via interconnections in 3-D packages using a single via structure with embedded capacitor. The model of a single via was extracted based upon the EM simulations of a test structure, in which the via was landed at an internal capacitance layer within the multi-layer LCP or printed circuit board (PCB) substrate. The objective for the single via modeling is to realize a simplified model that can be used for circuit simulation.

Chapter V (also published in [3]) presents de-embedding transmission lines using a full-wave EM-simulated pad model. A novel de-embedding method using a full-wave

EM simulated pad model is proposed to de-embed the pad parasitics from the test structure at high frequencies. The conventional de-embedding methods using the "open-short" approach and "symmetrical-line" approach are prone to error at high frequencies, while the EM-simulated-pad de-embedding method presented here shows improved accuracy and good agreement with the EM simulations result up to 67 GHz.

Chapter VI (also submitted for review in [4]) presents a low-power and low-voltage X-band SiGe HBT LNA. The power consumption of LNA in RF front-ends is a crucial design consideration in most wireless systems. In this dissertation, an ultra-low-power and low-voltage LNA is implemented in a 200 nm, 150 GHz peak f_T SiGe HBT BiCMOS process technology. For the first time, the performance of the LNA is measured both with the SiGe HBT biased in the conventional forward-active (FA) mode, as well as with the SiGe HBT biased in the weak-saturation (WS) mode, and the results are compared. In the WS mode, the LNA delivers a gain of 8.5 dB at 10 GHz with a noise figure (NF) of 3.1 dB, while consuming only 0.5 mW dc power, yielding a gain per dc power consumption figure-of-merit (FOM) of 17 dB/mW.

Chapter VII (also accepted in [5]) presents an X-band to Ka-band SPDT switch using 200 nm SiGe HBTs. The SPDT switch was fabricated using a 200 nm, 150 GHz peak f_T SiGe HBT BiCMOS process technology. The SPDT switch design used diode-connected SiGe HBTs in a series-shunt configuration to improve the switch bandwidth and isolation. Between 8 and 40 GHz, this SPDT switch achieves an insertion loss of less than 4.3 dB, an isolation of more than 20.3 dB, and a return loss of more than 9 dB.

Chapter VIII (also submitted for review in [6]) presents the packaging effects of multiple X-band SiGe LNAs embedded in an organic LCP Substrate. Interconnects in RF packages have a strong tendency to deteriorate RF performance, especially in high-frequency systems. In the dissertation, comparison is made between the wirebonded and embedded flip-chip packages. X-band SiGe LNAs are used to evaluate the performance of these interconnects. Measured results show that the embedded flip-chip packages have

better RF performance than the wirebonded packages for X-band applications. At 9.5 GHz, the flip-chip interconnects contribute only 0.4 dB of insertion loss, while the wirebond interconnects contribute 2.2 dB of insertion loss. The flip-chip and wirebond interconnects are modeled and validated against measured results from 8 to 20 GHz. For the first time, multiple die are put together in a single LCP package to compare the package effects and to demonstrate the feasibility of embedding multiple dies within a single package for highly integrated solutions.

Lastly, chapter IX concludes the dissertation with a discussion on possible future work. Figure 11 shows the block diagram of a T/R module, which outlines the research work from this dissertation. In addition, an MS thesis was completed in 2009 prior to this work [24].

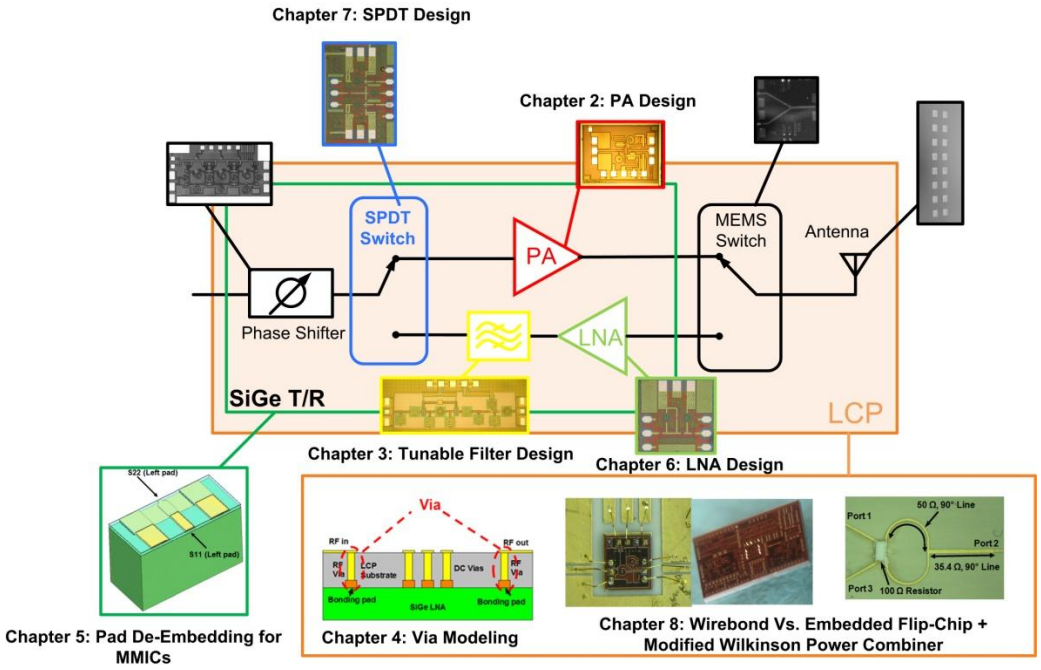


Figure 13: Block level of a T/R module depicting the outline of the research work

CHAPTER II

CASCODE X-BAND SIGE POWER AMPLIFIER

2.1 Introduction

As the speed of SiGe HBT increases, the breakdown voltage of the SiGe HBT inevitably decreases. The lack of available breakdown voltage makes it difficult to achieve a high output power in PA design. The voltage swing of a SiGe amplifier can be increased by using a cascode configuration [25].

Figure 14 shows the small-signal equivalent circuit for the transistors Q_1 and Q_2 in a cascode configuration.

The output resistance looking into the collector of Q_1 is given by

$$R_{o1} = r_{o1}, \tag{7}$$

and the input resistance looking into the emitter of Q_2 is

$$R_{i2} = r_{e2} = \frac{1}{1+\beta_2} r_{\pi 2} \approx \frac{r_{\pi 2}}{\beta_2}. \tag{8}$$

The voltage gain for the first stage is given as

$$A_{v1} = g_{m1}\left(R_{o1} // R_{i2}\right) \approx \frac{g_{m1}}{g_{m2}}. \tag{9}$$

The total output resistance of the cascode structure is given as

$$R_o \approx r_{o2}\left(1+\frac{g_{m2}r_{o1}}{1+\frac{g_{m2}r_{o1}}{\beta_2}}\right). \tag{10}$$

Since $g_{m2}r_{o1} >> \beta_2$ and $\beta_2 >> 1$, equation (10) can be simplified to

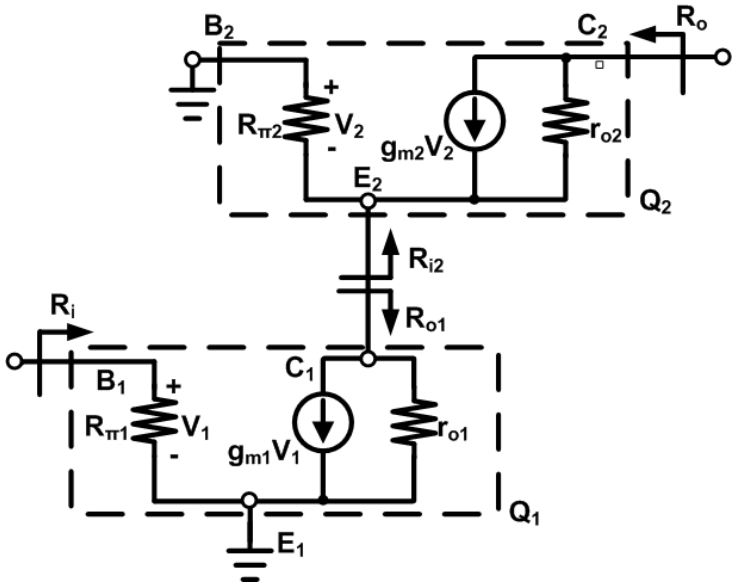


Figure 14: Small-signal equivalent circuit for the transistors Q_1 and Q_2 in a cascode configuration.

$$R_o \approx r_{o2}\beta_2 . \tag{11}$$

The total transconductance of the cascode structure is given by

$$G_m = g_{m1} . \tag{12}$$

Thus, from (11) and (12), the total voltage gain A_v for the cascode structure can be expressed as

$$A_v \approx G_m R_o \approx g_{m1} r_{o2} \beta_2 . \tag{13}$$

Through (13), it can be shown that the magnitude of the maximum available voltage gain of a cascode pair is higher by a factor β_2 than for the case of a single transistor. In addition, the cascode configuration helps to minimize the Miller effect and improves the isolation between the input and the output of the amplifier.

2.2 Measurement Results

In this work, an X-band PA was fabricated using 130 nm SiGe HBT BiCMOS technology (IBM 8HP). The X-band PA used a cascode configuration as shown in Figure 15. The transistors in the PA were biased at a current density based on the peak f_{max} condition. The PA input impedance was matched at the S_{11} conjugate for maximum gain condition. The PA output impedance was matched using the load-pull technique for maximum output power (P_{out}) [26]. The matching networks were implemented using the resistor-inductor-capacitor (RLC) elements. The device sizes for the cascode PA are described in Table 2.

The PA was measured on-wafer using ground-signal-ground (GSG) coplanar microwave probes. Agilent E8361C Vector Network Analyzer (VNA) was used for the S-parameter measurements and calibrated through the thru-reflect-line (TRL) standard to account for the cable losses.

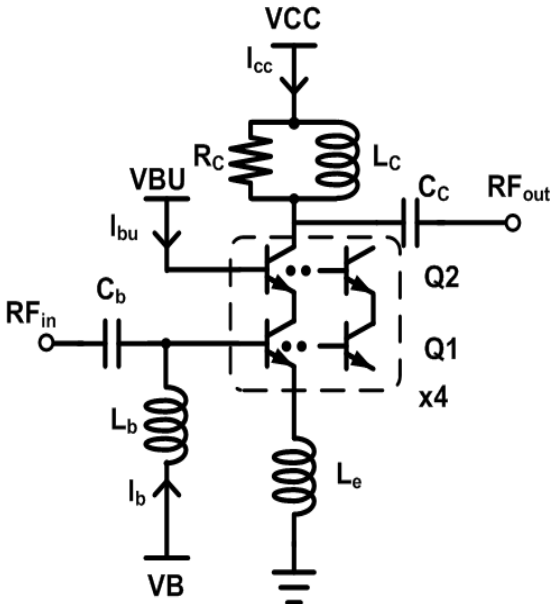


Figure 15: Schematic of the X-band PA.

Table 2: Device sizes for the X-band PA.

Parameter	Device Sizes
L_c	799.14 pH
L_b	880.62 pH
L_e	55 pH
R_c	800 Ω
C_b	242.40 fF
C_c	299.95 fF
Q_1 (High-speed)	0.12 x 6 x 4 μm
Q_2 (High-breakdown)	0.12 x 8 x 8 μm

Figure 16 shows the photomicrograph of the PA die. The total die area including the bond pads is 590 x 940 μm^2. The PA operates at VCC = 5 V, VBU = 1.9 V, and VB = 0.85 V. The total power dissipation for the small-signal gain is about 35 mW. Figure 17 shows the measured S-parameters of the X-band SiGe PA. At 9.5 GHz, the PA achieves a gain of 15.4 dB and return loss of more than 5 dB.

The output third-order intercept point (OIP_3) and the output-referred 1-dB gain compression point (P_{1dB}) are measured to evaluate the linearity of the PA. Figure 18 plots the measured OIP_3 for a two-tone test. The extrapolated OIP_3 is 25.7 dBm, with the fundamental frequency set at 9.5 GHz and frequency spacing for the two-tone set at 8 MHz. At 9.5 GHz, the PA has an output P_{1dB} of 16 dBm, an output P_{sat} of 19 dBm, and a peak power-added-efficiency (PAE) of 18.5%, as shown in Figure 19.

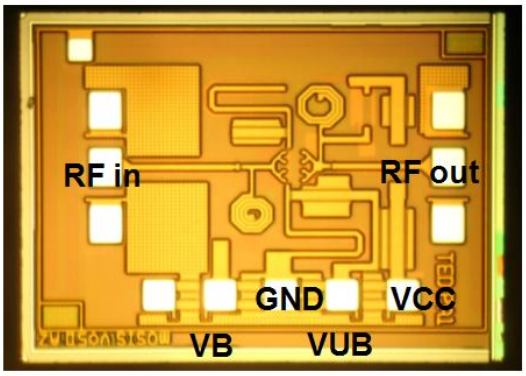


Figure 16: Photograph of the fabricated X-band SiGe PA.

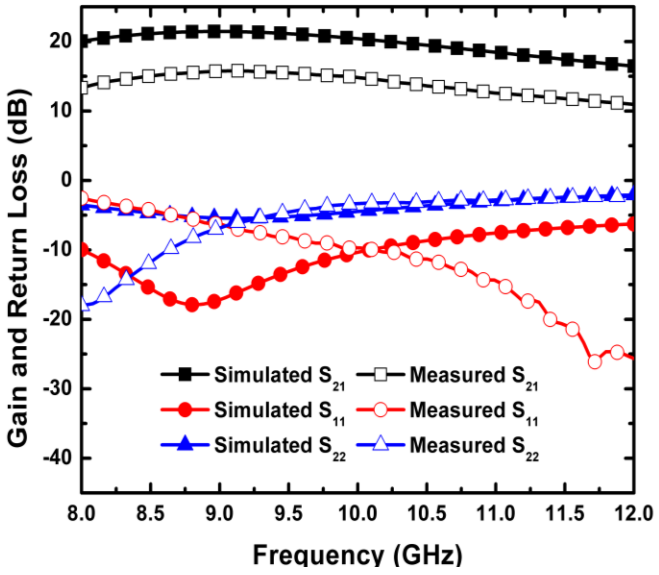


Figure 17: Measured S-parameters of the X-band SiGe PA.

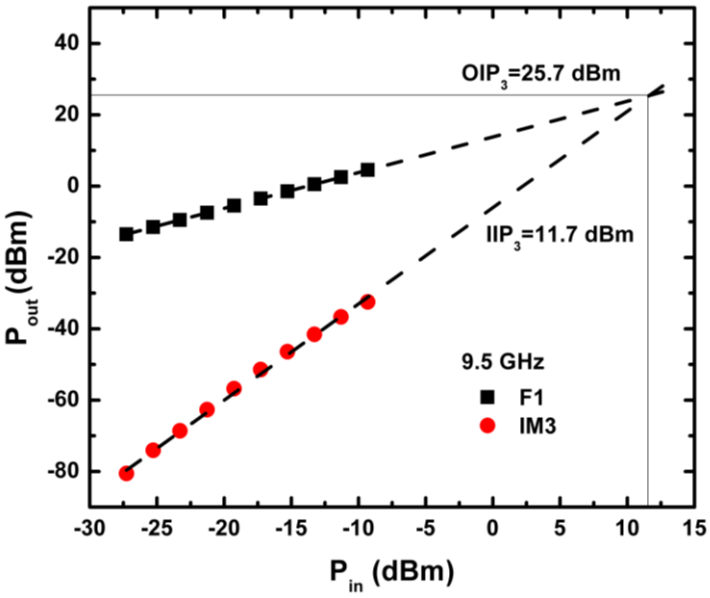


Figure 18: Measured third-order intercept point.

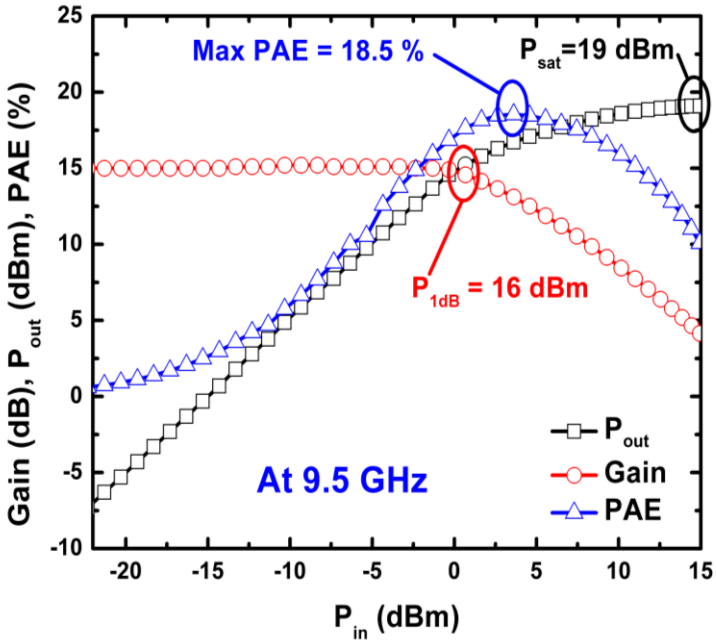


Figure 19: Measured gain, output P_{1dB}, max *PAE*, and output P_{sat} at 9.5 GHz.

Table 3 shows a comparison of the PA with other SiGe PAs. Two figure-of-merits (FOMs), FOM1 and FOM2, are used to benchmark the X-band PA as listed in Table 3. The FOM1 and FOM2 are expressed as follows:

$$FOM1 = \frac{P_{sat}(mW)}{Area(mm^2)}\ , \tag{14}$$

and

$$FOM2 = \frac{Gain(Mag) \cdot P_{sat}(mW)}{Area(mm^2)}\ . \tag{15}$$

The FOM1 normalizes the P_{sat} with respect to the size of the die [27], while FOM2 takes the PA gain into account. As shown in Table 3, the PA presents in this dissertation has the highest FOM2 as compared to other SiGe PAs.

2.3 Summary

An X-band PA was designed using 130 nm SiGe HBT BiCMOS technology. The X-band PA used a cascode configuration to increase the breakdown voltage so that the maximum output power can be achieved. At 9.5 GHz, the X-band PA has a gain of 15.4 dB, a return loss of more than 5 dB, an output P_{1dB} of 16 dBm, an output P_{sat} of 19 dBm, and a peak PAE of 18.5%.

Table 3: Comparison with other SiGe PAs.

	Frequency (GHz)	Gain (dB)	P_{sat} (dBm)	PAE (%)	N[++]	Area (mm^2)	FOM1 (mW/mm^2)	FOM2 (mW/mm^2)	Technology
This Work	**9.5**	**15**	**19**	**18.5**	**1**	**0.55**	144	**812**	**130 nm SiGe**
[25]+	8.5~10.5	11	29.3	18	4	4.5	243	671	130 nm SiGe
[28]	8.4	8.7	23	12	1	0.75	266	724	SiGe/Si HBT
[29]	8.5~10.5	12.2	21.2	27.4	1	0.86	153	624	250 nm SiGe
[30]	7-18	17.5	17.5	10.1	2	0.72	78	585	350 nm SiGe
[31]	1-12	12	16	10	4	2.1	19	75.5	250 nm SiGe

[+] With off-chip matching [++] Number of stages

CHAPTER III

MONOLITHIC X-BAND TUNABLE BANDPASS FILTER

3.1 Introduction

A low-cost, highly integrated, single-chip RF front-end is an attractive solution for modern communication systems. RF filters are essential components in communication systems because they help to improve the sensitivity of a receiver by suppressing out-of-band interference. At present, most filters used at low frequencies (< 2 GHz) are implemented using off-chip lumped elements, while at high frequencies (> 3 GHz), planar filters are used instead [32,33]. This usually leads to a bulky filter design, making miniaturization difficult to realize. Much effort is required to integrate these filters with the rest of the RF blocks in the system.

With the advancement of silicon technologies, many millimeter-wave on-chip filters have been proposed recently [34,35,36]. For multiband receivers, on-chip tunable filters can be implemented to replace switched filter banks [37], in order to reduce the number of filters used, the cost, and the size of the system, as shown in Figure 18. SiGe HBT BiCMOS technology [38] offers a highly-integrated mixed signal solution that enables one to integrate all of the RF blocks on a single die, resulting in system miniaturization, which helps to reduce the production cost, simplify the integration process, and improve the overall system reliability. Besides offering integration advantages, SiGe HBT BiCMOS technology also enables circuits requiring robust operation in extreme environments, such as conditions found in space or earth orbit, where operating temperatures can be as low as 90 K and radiation exposure is unavoidable [39].

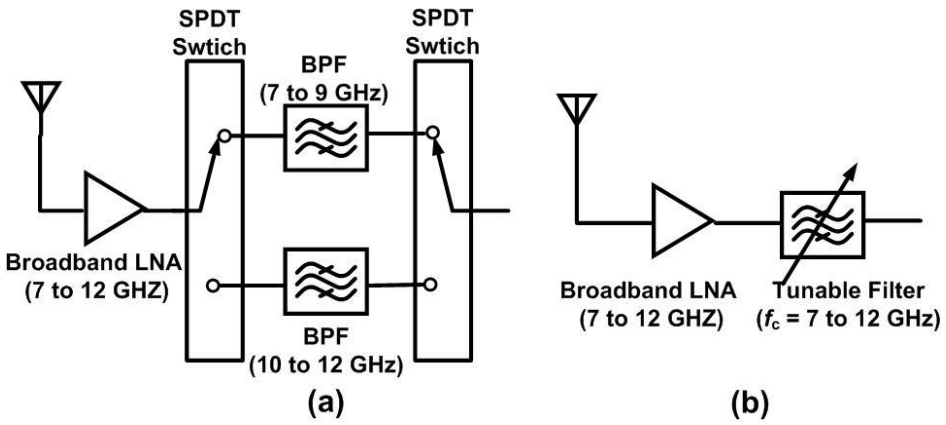


Figure 20: Multiband receiver: (a) switched filter bank and (b) tunable filter.

In the dissertation, a monolithic X-band active tunable bandpass filter (BPF) is implemented in a 130 nm SiGe BiCMOS process technology (IBM 8HP) for the first time. The integration capabilities offered by the SiGe HBT BiCMOS technology enable a SiGe filter to be integrated with a SiGe LNA, which improves the overall performance by minimizing the insertion loss and the NF [40,41,42,43]. Compared to the previous work, the active X-band tunable filter presented in this dissertation consumes a minimal *dc* power (P_{dc}) of 2.75 mW, has an insertion loss of less than 1.2 dB and a low NF of less than 3.8 dB, with the center frequency (f_c) that can be tuned from 8.3 to 11.7 GHz. In addition, the temperature effects on the filter S-parameters are presented.

3.2 Filter Design

The active tunable BPF consists of two stages: the gain stage and the filter stage. The gain stage consists of a SiGe LNA and the filter stage consists of a tunable BPF implemented at X-band using the passive components found within SiGe HBT BiCMOS technology. The schematic of the active tunable BPF is shown in Figure 21.

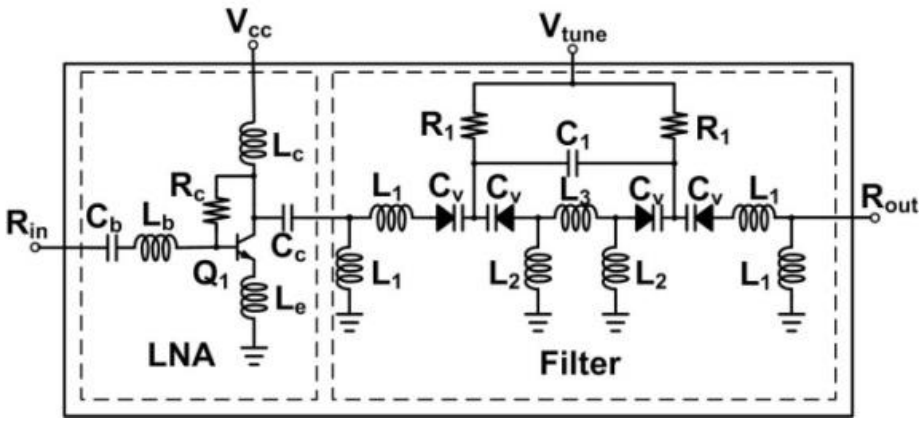


Figure 21: Schematic of the active tunable SiGe BPF.

The SiGe LNA is implemented in a single stage common-emitter (CE) configuration with a resistive feedback topology to broaden its bandwidth [44]. Figure 22 shows the simulated S-parameters of the LNA. At X-band at room temperature, the SiGe LNA was simulated to have a gain of more than 9 dB, a return loss of more than 8 dB, and a NF of less than 2 dB. Table 4 shows the components used for the SiGe LNA.

The filter [45] is based on two tank circuits coupled by one inductor, L_3. The input and output tank circuits consist of inductors L_2, L_4, and a varactor, C_v. The inductor L_1 is mainly used to match the filter to 50 Ω. The resistor R_1 is used as a RF choke. A *dc* voltage (V_{tune}) is used to vary the varactor capacitance for tuning the filter center frequency (f_c). The simulation results shows that the varactor capacitance decreases with voltage and increases with temperature, as shown in Figure 23.

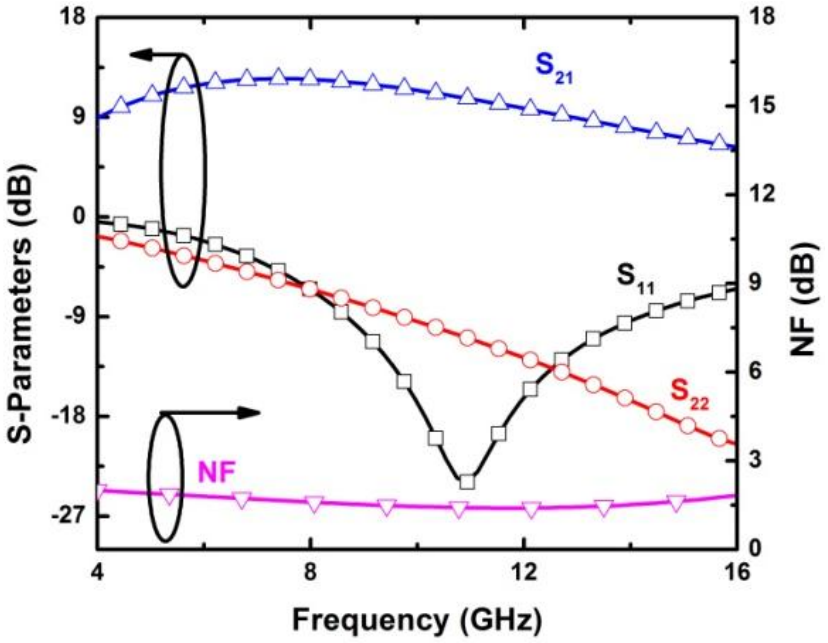


Figure 22: S-parameters and noise figure simulations of the SiGe X-band LNA.

Table 4: Components for the SiGe LNA.

Component	Value
L_b (nH)	1.37
L_c (nH)	1
L_e (pH)	272
R_1 (kΩ)	5
R_c (kΩ)	17
C_b (pF)	1
C_c (fF)	491
Transistor (μm^2)	18 x 0.12

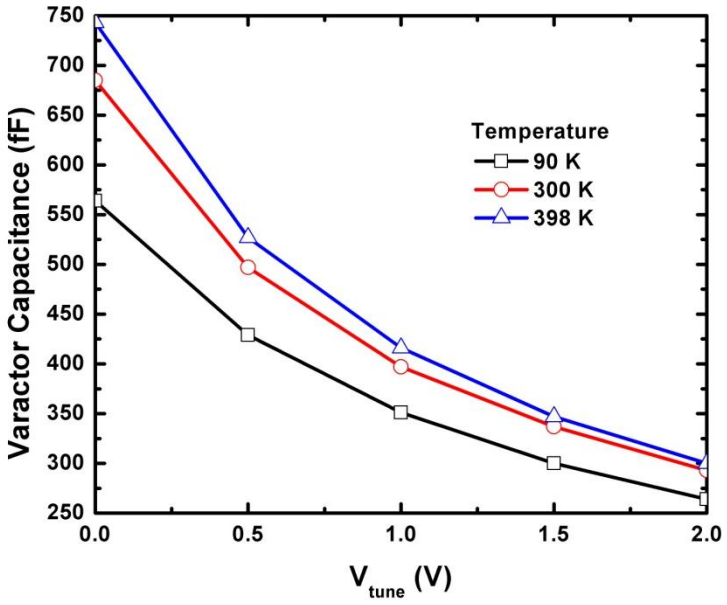


Figure 23: Varactor capacitance vs. V_{tune}.

The BPF can be analyzed using the Y-Δ transformation, as shown in Figure 24. The π-network in the BPF consists of the following impedances, Z_1, Z_2, and Z_3. The impedances are given as

$$Z_1 = \frac{1}{j2\pi f C_v}, \tag{16}$$

$$Z_2 = j2\pi f L_4 , \tag{17}$$

and

$$Z_3 = j2\pi f L_3 . \tag{18}$$

Through the Y-Δ transformation,

$$Z_4 = \frac{Z_2 Z_3}{2Z_2 + Z_3}, \tag{19}$$

$$Z_5 = \frac{Z_2{}^2}{2Z_2 + Z_3} , \tag{20}$$

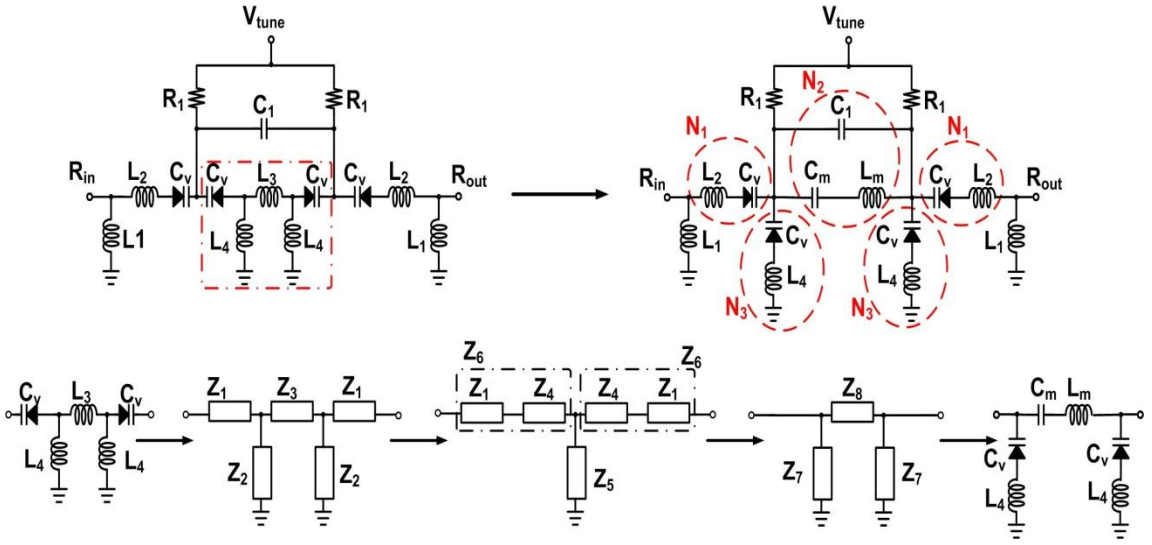


Figure 24: Circuit analysis of the filter stage.

and

$$Z_6 = Z_1 + Z_4 . \tag{21}$$

Impedances Z_5 and Z_6 are then converted from the Y network into the Δ network using Y-Δ transformation, where

$$Z_7 = Z_1 + Z_2 \tag{22}$$

and

$$Z_8 = 2Z_1\left(1+\frac{Z_3}{Z_2}\right)+Z_3\left[1+\frac{Z_1^2}{Z_2^2}\left(2\frac{Z_2}{Z_3}+1\right)\right]. \tag{23}$$

From (23), the impedance Z_8 is translated into its equivalent capacitance and inductance, C_m and L_m, respectively, where

$$C_m = \frac{C_v}{2\left(1+\frac{L_3}{L_4}\right)} \tag{24}$$

and

$$L_m = L_3\left[1+\frac{1}{(2\pi f)^4 L_4^2 C_v^2}\left(2\frac{L_4}{L_3}+1\right)\right]. \tag{25}$$

In Figure 24, there are three resonators, N_1, N_2, and N_3 in the filter. At the resonant frequency, N_2 and N_3 create two transmission zeros at frequencies F_{low} and F_{high}, respectively, while N_1 is used to create a bandpass response between F_{low} and F_{high}. The resonant frequencies can be expressed as

$$F_{low} = \frac{1}{2\pi}\sqrt{\frac{C_1 + C_m}{C_m C_1 L_m}}, \tag{26}$$

$$F_{high} = \frac{1}{2\pi\sqrt{C_v L_4}}, \tag{27}$$

and

$$F_{bandpass} = \frac{1}{2\pi\sqrt{C_v L_2}}. \tag{28}$$

Through (24) to (28), the components in the tunable BPF can be determined. Table 5 shows the components used for the tunable X-band filter.

Figure 25 shows the simulated S-parameter results of the filter stage. When V_{tune} is set from 0 to 2.0 V, the filter center frequency (f_c) shifts from 8 to 11 GHz. At bandpass, the insertion loss is about 8 dB and the return loss is more than 10 dB.

Table 5: Components for the filter stage.

Component	Value
C_1 (pF)	3.62
C_v (fF) [a]	685 ~ 293
L_1 (pH)	335
L_2 (pH)	335
L_3 (pH)	976
L_4 (pH)	280
R_1(kΩ)	5

[a] V_{tune} ranges from 0 to 2.0 V at 300 K.

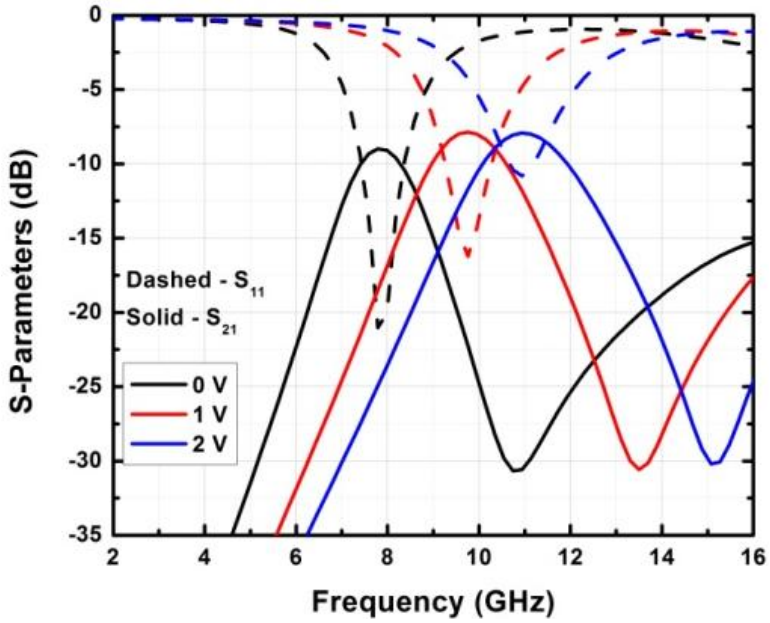


Figure 25: Simulated S-parameters of the filter stage.

When the gain stage is cascaded with the filter stage, the overall bandpass gain improves. As shown in Figure 26, the simulated results show that the filter bandpass gain is more than 3 dB and the return loss is more than 8 dB.

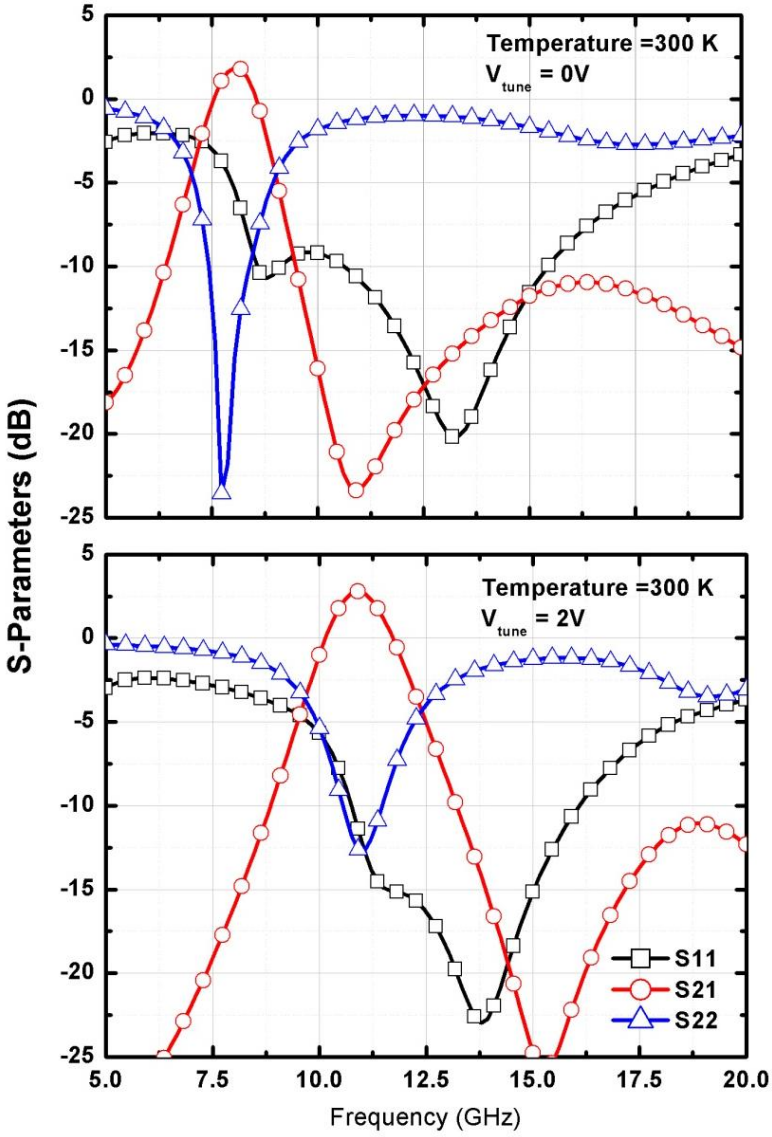


Figure 26: Simulated S-parameters for the active tunable SiGe BPF.

3.3 Measurement Results

The filter was fabricated using a 130 nm, seven-metal-layer, commercial-available, SiGe HBT BiCMOS process technology (IBM 8HP). Including the bondpads, the size of the filter is 1.85 x 0.70 mm^2 in size. S-parameter measurements were

performed using an Agilent E8363B Vector Network Analyzer (VNA) with the Thru-Reflect-Line (TRL) calibration from 5 to 20 GHz. Figure 27 shows the photomicrograph of the active tunable SiGe filter.

The filter was designed to operate with a supply voltage as low as V_{cc} = 1.0 V and I_c = 2.75 mA, yielding a total power dissipation of 2.75 mW. Figure 28 shows the measured S-parameter results of the filter. The filter has an insertion loss of less than 1.2 dB. The filter tunes is at 8.3 and 11.7 GHz when Vtune is set at 0 and 2 V, respectively (41% tuning ability). The measured S-parameter results of the filter are tabulated in Table 6.

The discrepancies between the simulated and measured results can be attributed to the inaccuracies in the design kit varactor model. In addition, on the layout, metal-fills were placed closer to the inductors than intended. This may reduce the actual inductances on die and affect the 50 Ω impedance match [46]. As the frequency increases, the Q-factors of the inductors decrease and widen the filter bandwidth.

The NF was measured using the noise figure measurement personality in an Agilent E4446A Spectrum Analyzer. Figure 29 shows the simulated and measured NF. The average noise figure is about 3.66 dB across X-band. The difference between the simulated and the measured NF is because of the degradation in the measured S_{21}, which increases the overall noise figure.

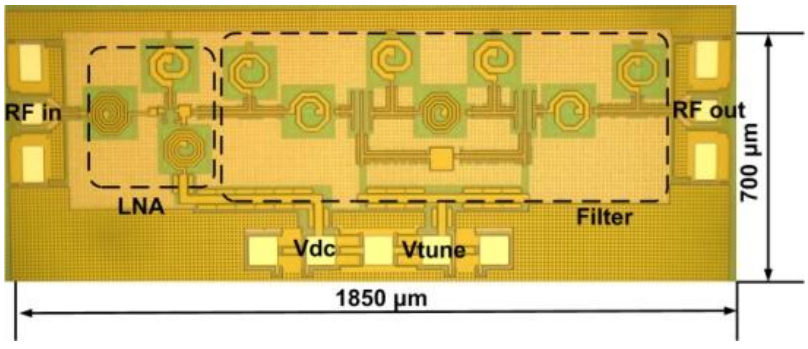


Figure 27: Photomicrograph of the active tunable SiGe BPF.

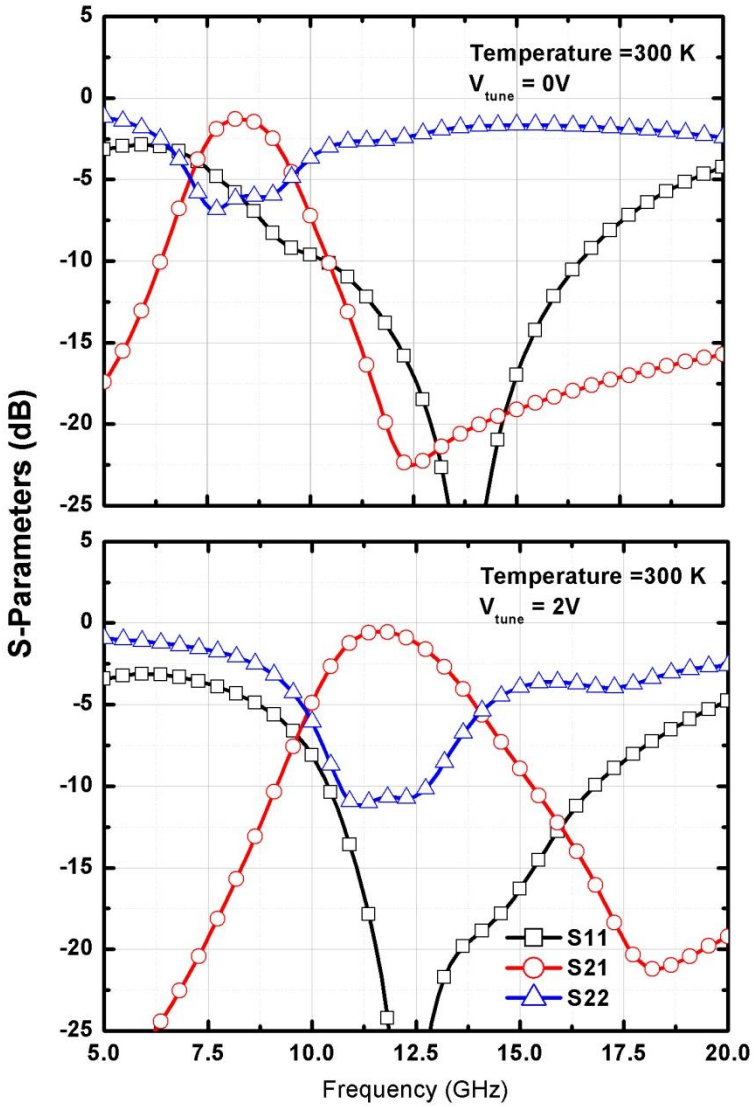


Figure 28: Measured S-parameters of the active tunable SiGe BPF at 300 K.

Table 6: S-parameter results of the filter at 300 K.

V_{tune}	0 V	2 V
f_c (GHz)	8	11
S_{21} (dB)	-1.2	-0.1
S_{11} (dB)	-5.2	-12
S_{22} (dB)	-6	-8.4
3-dB BW (GHz)	2.0	3.0
Fractional BW (%)	25	27

BW - Bandwidth

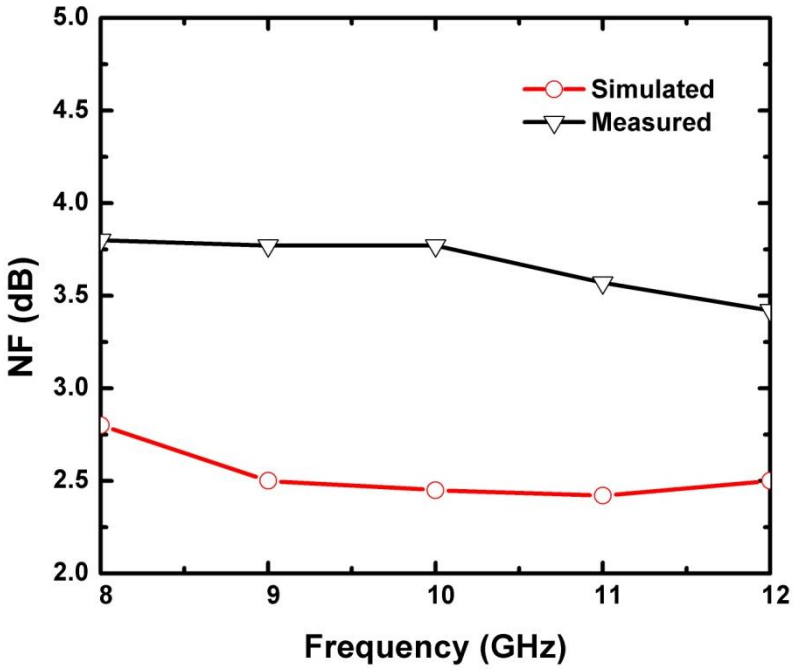


Figure 29: Simulated and measured noise figure of the active tunable SiGe BPF.

As the RF input signal increases, the varactor capacitance begins to vary, causing the filter response to become increasingly nonlinear. A two-tone, third-order interception point (IIP3) measurement was performed on the filter using the Agilent E4446A Spectrum Analyzer. Two tones with the same amplitude were applied to the filter at the frequencies 8.300 GHz and 8.308 GHz. The worst-case IIP_3 occurs when the V_{tune} is set at 0 V, because the varactor has a higher rate of change in its capacitance at lower V_{tune}. The worst-case measured IIP_3 of the filter is -7.1 dBm, as shown in Figure 30. The worst-case measured input-referred 1-dB compression point (P_{1dB}) of the filter is about -13.5 dBm, as shown in Figure 31.

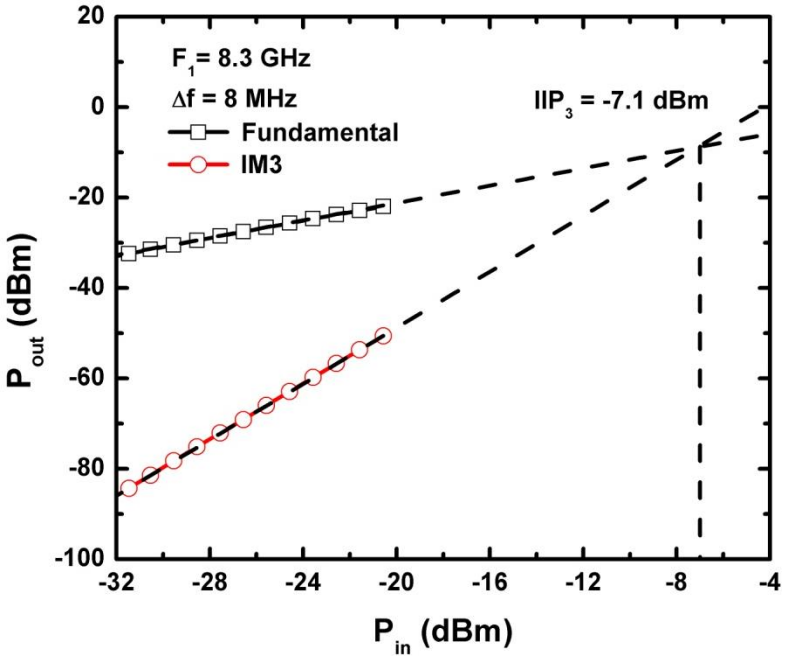


Figure 30: Worst-case IIP_3 measured result.

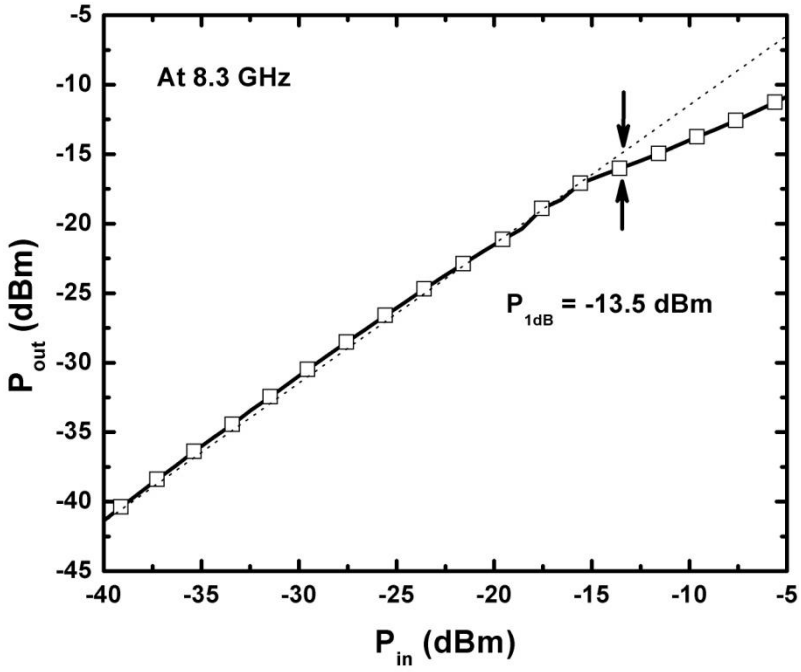


Figure 31: Worst-case P_{1dB} measured result.

3.4 Temperature Effects

The filter was measured across temperatures ranging from 90 K to 398 K. For the cryogenic measurement (90 K), the filter was measured using a custom on-wafer cryogenic probe station. Figure 32 shows the measured S-parameters of the filter at cryogenic temperature. The filter has an insertion loss of less than 0.2 dB. The filter f_c is at 9.1 and 12 GHz when V_{tune} is set at 0 and 2 V, respectively (31.9% tuning ability). The high temperature measurement (398 K) was performed using a Temptronic digitally controlled hot chuck. Figure 33 shows the measured S-parameters of the filter at high temperature. The filter has an insertion loss of less than 3.5 dB. The filter f_c is at 7.8 and 11.2 GHz when V_{tune} is set at 0 and 2 V, respectively (43.6% tuning ability). Table 7 summarizes the measured S-parameter results of the filter across temperatures.

The filter S_{21} changes with the temperatures. At 90 K, the filter response improves by more than 1 dB and at 398 K, the filter response degrades by less than 2.7 dB. The changes in S_{21} response are the results of the temperature-induced changes in the SiGe HBT used in the LNA. At lower temperatures, the SiGe HBT has much higher current gain [47], while at higher temperatures, the SiGe HBT has a decreased current gain [48].

In addition, the filter f_c increases as the temperature decreases. As shown in Figure 23, the varactor capacitance decreases as the temperature decreases. At lower temperatures, the varactor capacitances resonate with the inductors at higher frequencies, which shift the f_c to higher frequencies, and vice versa at higher temperatures. At 90 K, the f_c increases by less than 0.8 GHz and at 398 K, the f_c decreases by less than 0.5 GHz. The frequency shift in the f_c can be offset by applying a lower V_{tune} at the lower temperature and vice versa at the higher temperature, since the filter response can be tuned continuously from 0 V onwards.

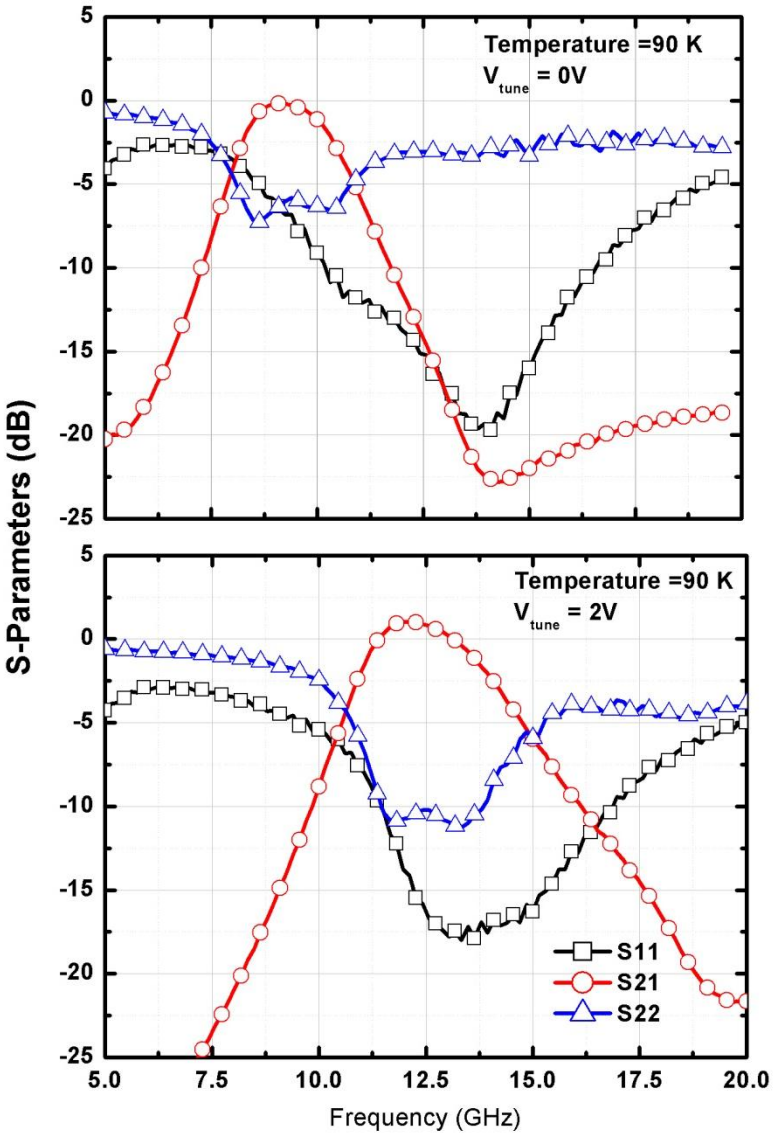


Figure 32: Measured S-parameters of the active tunable SiGe BPF at 90 K.

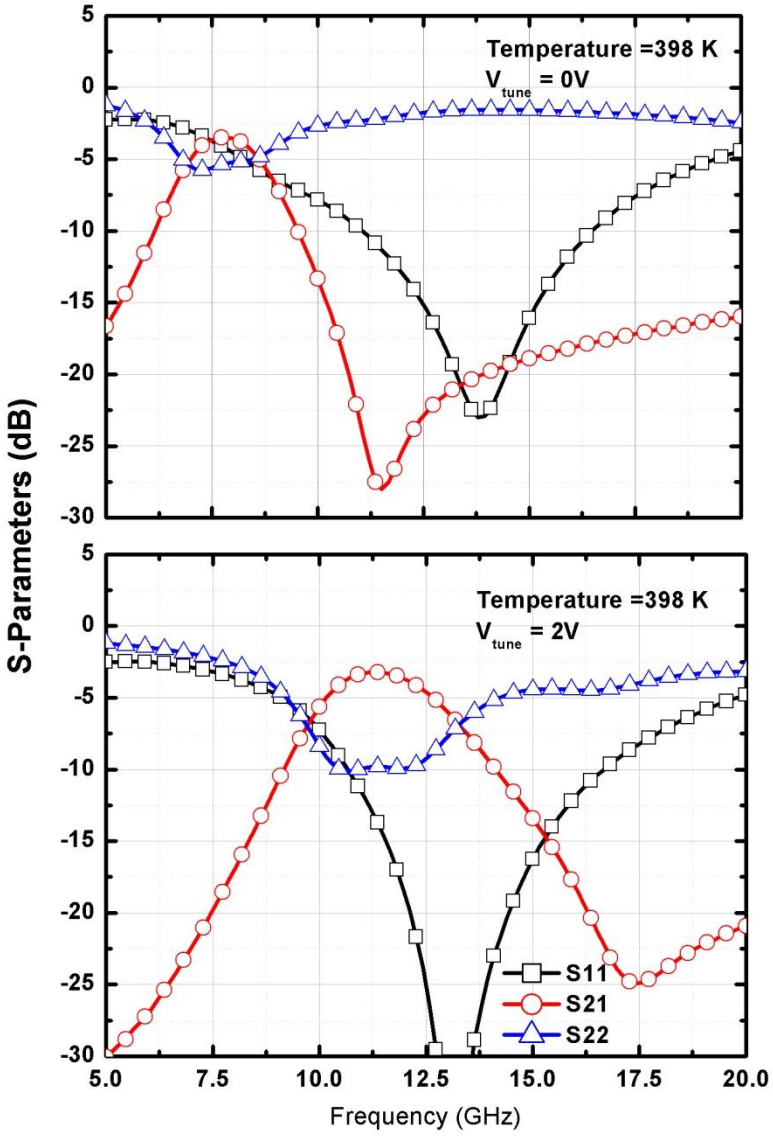


Figure 33: Measured S-parameters of the active tunable SiGe BPF at 398 K.

Table 7: S-parameter results across temperatures.

Temperature (K)	90		398	
V_{tune} (V)	0	2	0	2
f_c (GHz)	9.1	12	7.8	11.2
S_{21} (dB)	-0.2	1	-3.5	-3.2
S_{11} (dB)	-6.4	-14.2	-4.3	-13.7
S_{22} (dB)	-6.4	-10.8	-5.3	-9.8
3-dB BW (GHz)	2.3	2.9	2.2	3.1
Fractional BW (%)	25.3	24.2	28.2	27.7

BW - Bandwidth

3.4 Benchmarking

Table 8 shows a comparison between different active on-chip filters and the present work. Two figures-of-merits, *FOM1* and *FOM2*, are used to benchmark the filters listed in Table 8. *FOM1* is defined as

$$FOM1 = \frac{Q_{filter} \cdot S_{21}(Mag)}{P_{dc}(mW) \cdot NF(Mag)}, \tag{29}$$

where Q_{filter} is the ratio of the f_c and the 3-dB bandwidth, S_{21} is the filter bandpass gain in absolute, P_{dc} is the *dc* power consumption expressed in milliwatts, and NF is the noise figure in absolute. This figure-of-merit favors filters with low insertion loss and high Q_{filter} with respect to the P_{dc} and NF.

FOM 2 is given as

$$FOM2 = \frac{Q_{filter} \cdot S_{21}(Mag) \cdot P_{1dB}(mW) \cdot f_c(GHz)}{P_{dc}(mW) \cdot NF(Mag)}, \tag{30}$$

where the f_c and power handling (P_{1dB}) of the filter are also taken into consideration [42]. In both cases, a large figure-of merit is better.

TABLE 8: Comparison between other active filters.

Reference	This Work	[42]	[49]	[50]	[51]	[52]	[53]
Process	130 nm SiGe HBT	250 nm CMOS	180 nm CMOS	180 nm CMOS	180 nm CMOS	150 nm GaAs pHEMT	65 nm CMOS
Size (mm^2)	1.29	0.53	1.21	0.13^{+}	1.08	1.00	0.07^{+}
$f_c$$^{++}$ (GHz)	11.7	3.84	2.03	**22.7**	6.02	21.5	1
Gain (dB)	-0.5	**12**	0	0.0	-2.2	-2	-2
P_{1dB} (dBm)	-11.0	-18.0	-6.6	-7.65	-15.2	-19	**2**
P_{dc} (mW)	**2.75**	10.8	17	3.3	5.4	50.0	16
NF (dB)	**3.66**	20	15	14	11.4	17	5.5
Tuning Range (GHz)	**3.4**	1.9	0.06	0^{+++}	0^{+++}	2	0.9
3-dB Bandwidth (%)	27.2	0.94	6.5	7.4	18.94	4.2	3.5
***FOM1* (mW^{-1})**	**0.56**	0.39	0.03	0.16	0.06	0.01	0.4
***FOM2* (GHz)**	0.52	0.02	0.01	**0.64**	0.01	0.02	0.63

+ without bondpads; ++ Maximum f_c; +++ Non-tunable

Through Table 8, the filter presented in this work is shown to achieve the highest published *FOM1*. The filter uses the least P_{dc}, has a wide tuning range, and has the lowest NF, as compared to the other filters.

3.5 Summary

This dissertation has demonstrated an X-band tunable active BPF implemented in a SiGe HBT BiCMOS technology. The filter uses low P_{dc} of 2.75 mW, has an insertion loss of less than 1.2 dB, a low NF of less than 3.8 dB, and a wide tuning range from 8.3 to 11.7 GHz. S-parameters were measured from 90 to 398 K. The filter has a better insertion loss performance at lower temperature. As compared to room temperature measurements, the filter bandpass gain improves by more than 1 dB at 90 K and degrades by less than 2.7 dB at 398 K. This work has demonstrated that the SiGe HBT BiCMOS technology has the potential to develop highly integrated tunable filters that can lead to many opportunities for Si-based RF SOC solutions.

CHAPTER IV

EXTRACTION OF EQUIVALENT CIRCUIT MODEL FOR VIA INTERCONNECTION

4.1 Introduction

There is a continual driving force for a low cost packaging solution that can lead to higher system functionality with reduced overall size and weight. Conventional packages which use ribbon or wire bonding [15] as interconnections tend to introduce larger parasitic which in turn degrade the system performance, particularly at higher frequencies [16]. Therefore, these structures do not provide an efficient packaging solution for many high-speed electronic systems.

Novel organic materials such as LCP have been used for MMIC packaging because of its excellent high-frequency electrical properties, including low dielectric constant and low loss tangent [54]. LCP can be used as a dielectric material to de-embed the MMIC with the interconnecting vias replacing the ribbon and wire bond in the package [55]. This packaging approach offers lower parasitic interconnects and potentially enables the 3-D System-on-Package integration as depicted in Figure 34. Photo-micrograph of an X-band SiGe low noise amplifier (LNA) die is shown in Figure 324. The vias in the LCP serve as Z-interconnects to the LNA bond pads, as shown in Figure 34b where a 2 mil LCP layer is bonded to the LNA and vias were drilled through the LCP to land on the bond pads in the LNA. Figure 34c shows the cross-sectional view of an all LCP 3-D package with the embedded LNA. The details of the design and measured results of the LCP-packaged SiGe LNA can be found in [55].

Clearly, modeling of the via interconnection in 3-D packaging scheme is an important issue to address in the overall package design, as it is used to route among

active and passive components which are embedded inside the multi-layer circuit board. One way to model the via interconnections is to perform a full-wave EM simulation for the package. However, this is time consuming and increases the design complexity. Hence, it is highly desirable to implement an equivalent circuit model for the via to be used in the circuit simulations.

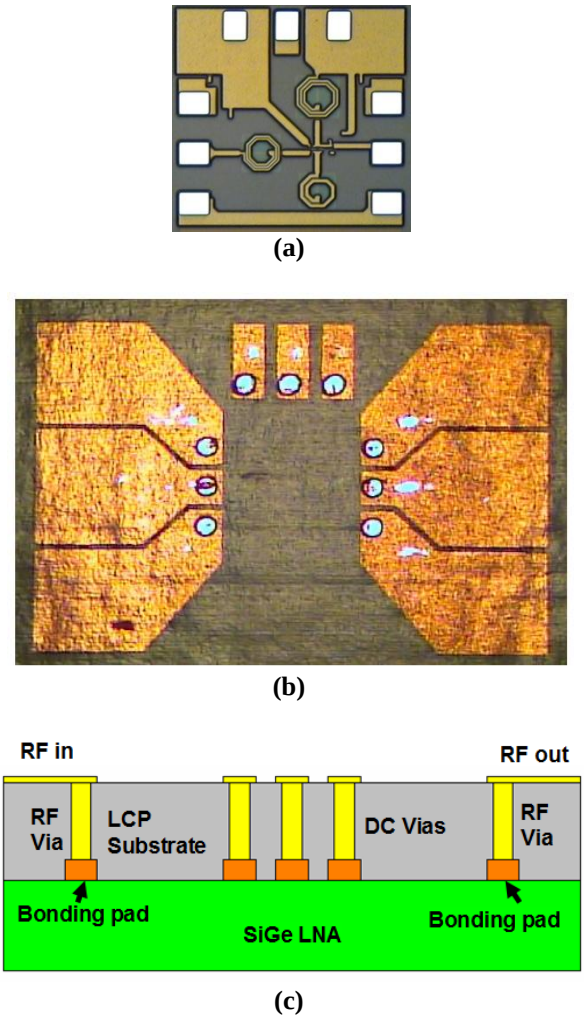


Figure 34: (a) Photograph of an X-band SiGe LNA die, (b) top view of the package on the SiGe LNA, and (c) cross-sectional view of the LCP substrate laminated on the top of the LNA.

Many test structures have been reported to extract the electrical equivalent circuit of via interconnections. Very often, such test structures need at least two sets of via interconnections in which the S-parameter matrix for a single via is extracted from the S-parameter matrix of the entire structure, under the assumption that the two sets of via are identical [56,57,58]. In this dissertation, a single via structure consists of embedded capacitors in a multi-layer PCB is used to extract the via parasitic model [59]. The approach of using a single via structure with embedded capacitors to extract the via parasitics is straightforward, as the EM simulation for a single via takes shorter time to run and minimal effort is required to design the embedded capacitors which can be fabricated using standard PCB process.

A single via interconnect model has been reported by Madou and Martenes [59] in a multi-layer PCB platform. However, the authors used 100 micron thick organic PCB layer with a dielectric constant of 6.5, yielding a capacitance density of 0.08 nF/cm^2. The measurement range was 300 KHz to 4 GHz. In contrast, the embedded capacitance layer in this study is relatively thin (16 micron) with a much higher capacitance density of 1.1 nF/cm^2. Moreover, the frequency domain in our study is up to 12 GHz, which would conceivably surpass the self resonance frequencies of PCB compatible capacitors. For decoupling applications, a higher capacitance density is more desirable.

4.2 Modeling using Multi-Layer LCP Test Structure

A shunt capacitor to ground was formed by depositing a layer of 0.05 μm alumina on the ground plane with a layer of 3 μm thick copper on the top surface of the alumina. The capacitor was then laminated with LCP and a diameter 100 μm via hole was drilled in the LCP to expose the top copper layer of the capacitor. Metallization layers were then deposited on the via and transmission lines were patterned on the top of the LCP with the

via hole places at the center. Figure 35 shows the cross-sectional view of the via test structure.

Figure 36 shows the 3-D view of the test structure, which consists of a coplanar waveguide (CPW) transmission line with the signal line width of 108 μm and ground spacing of 62 μm. The via diameter for the test structure is 100 μm. The capacitance (C) for the test structure can be determined by the thickness and the radius of the alumina according to (31)

$$C = \varepsilon_r \varepsilon_o \frac{\pi (radius)^2}{Thickness} \ . \tag{31}$$

The dielectric constant (ε_r) of the alumina is 9.9, the dielectric permittivity (ε_o) is 8.85×10^{-12} F/m. The top electrode has a radius of 150 μm and the capacitance is calculated to be 125 pF.

For a via of 2 mil height and 100 μm diameter, the ideal S_{21} response is shown in Figure 37. However, the via is not an ideal interconnect and in reality, the capacitor resonates with the via parasitics. Actual response of the test structure is also shown in Figure 37. The difference between the actual and ideal result becomes larger at higher frequencies due to the via parasitics.

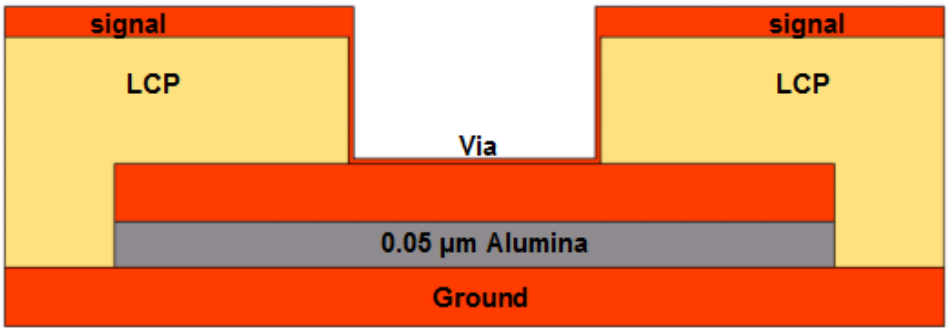


Figure 35: The cross-section of the test structure.

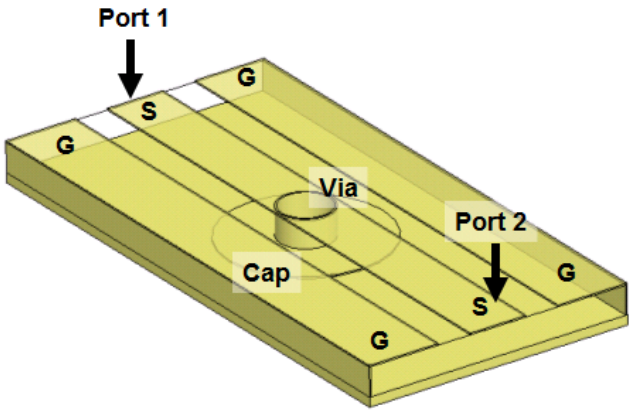


Figure 36: The 3-D view of the test structure.

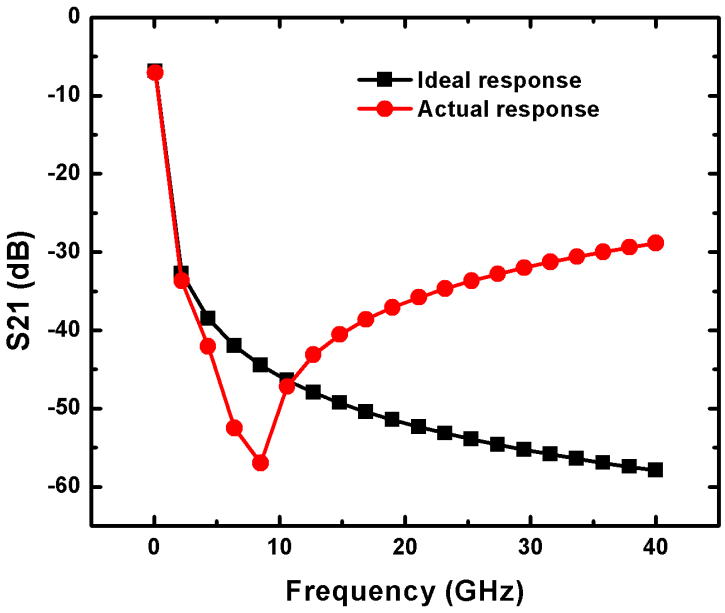


Figure 37: S_{21} of the test structure.

4.3 Parasitic Extraction

Using HFSS 3-D EM simulation, the two-port S-parameters of the single-via structure were extracted and translated into an equivalent π-circuit model, as shown in Figure 38. Z_{11}-Z_{12} represents the CPW line. Z_{12} represents the impedance which is caused by the via parasitics and the capacitor. Since the capacitance is known, the impedance of the via parasitics can be solved to derive the lump elements for the via model.

The relationship between Z_{12} and the S-parameter is given as,

$$Z_{12} = Z_0 \frac{2S_{12}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} \ . \tag{32}$$

Figure 39 shows the equivalent circuit model, which represents Z_{12}. *R* represents the parasitic resistance of the via, *L* represents the parasitic inductance of the via, and C_g represents the coupling between the via and the surrounding ground plane.

As the impedance Z_{12} is a complex number, the real and imaginary term are given in (33) and (34), respectively.

$$real = \frac{R(1-4\pi^2 fC_g L + \frac{C_g}{C+C_g}) + 2\pi fC_g R\left[2\pi fL - \frac{1}{2\pi f(C+C_g)}\right]}{(1+\frac{C_g}{C+C_g} - 4\pi^2 fC_g L)^2 + (2\pi fC_g R)^2}, \tag{33}$$

and

$$imag = \frac{\left[2\pi fL - \frac{1}{2\pi f(C+C_g)}\right](1-4\pi^2 fC_g L + \frac{C_g}{C+C_g}) - 2\pi fC_g R^2}{(1+\frac{C_g}{C+C_g} - 4\pi^2 fC_g L)^2 + (2\pi fC_g R)^2} \ . \tag{34}$$

Through (33) and (34), the lumped-element values, *R*, *L*, and C_g, of the via model can be determined. EM simulations had been performed for the test structure for different via heights. Table 9 summarizes the parasitics with the via height. Figure 40 shows how the parasitics vary as a function of via height.

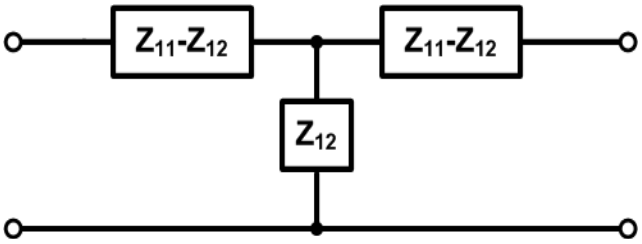


Figure 38: The equivalent π-circuit model.

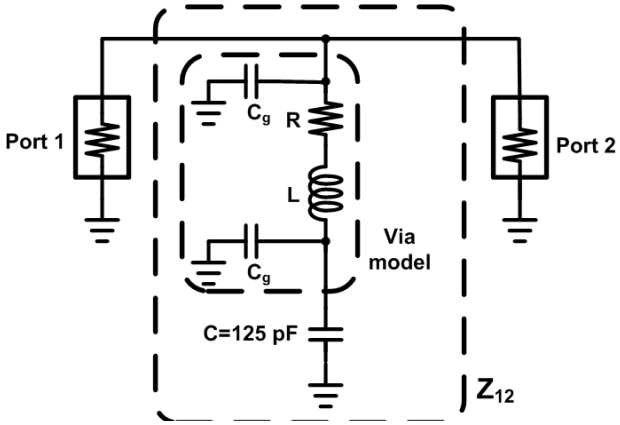


Figure 39: The equivalent circuit model for the via.

Table 9: Via parasitics for different via heights.

Via Height (mil)	*R* (Ω)	*L* (pH)	C_g (fF)
2	0	3.47	0
3	0	8.33	1.2
4	0.001	14.8	5
6	0.004	32.1	8
8	0.006	48.9	10
10	0.008	66	12.15

Based on Figure 40, the relationship between the via parasitics and the via height can be approximately expressed as

$$R = 0.0011H - 0.0028, \tag{35}$$

$$L = 8.0027H - 15.082, \tag{36}$$

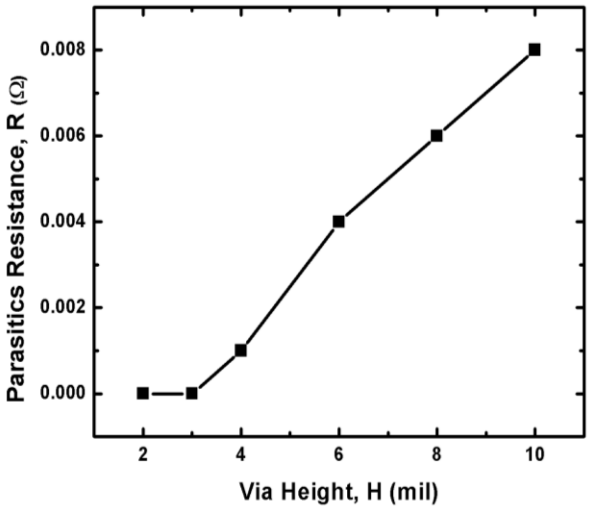
and

$$C_g = 1.5405H - 2.4126. \tag{37}$$

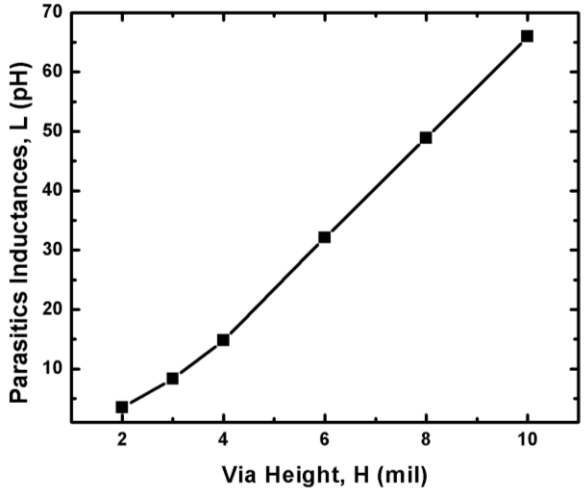
where R is in Ω, L is in pH, C_g is in fF, and H is in mil. Using (35)-(37), the values of the parasitic components of the via can be estimated.

4.4 Model and EM Simulation Verification

In HFSS 3-D EM simulations, a CPW line was connected to another CPW line through the via interconnect, as shown in Figure 41. For the model simulations, the equivalent circuit model for the via was extracted based on the EM simulated results of the single-via test structure. This model was then used for circuit simulation in ADS. Figure 42 shows the circuit simulation using the model. Figure 43 shows the EM and the model simulations results for different heights, 2, 6, and 10 mil.



(a)



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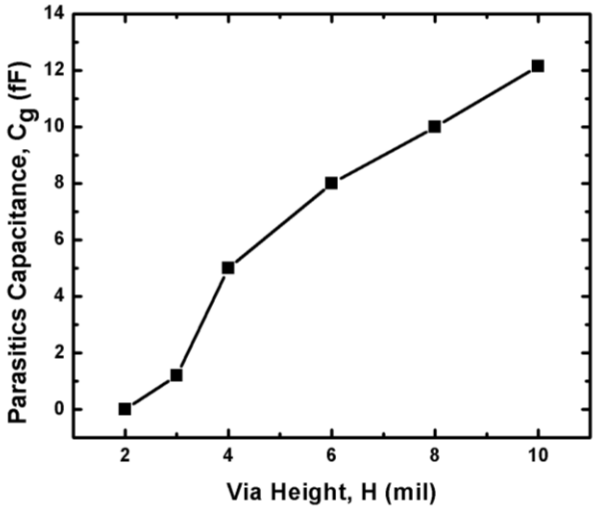


(c)

Figure 40: Parasitic values as a function of *H*: (a) *R*, (b) *L*, and (c) C_g.

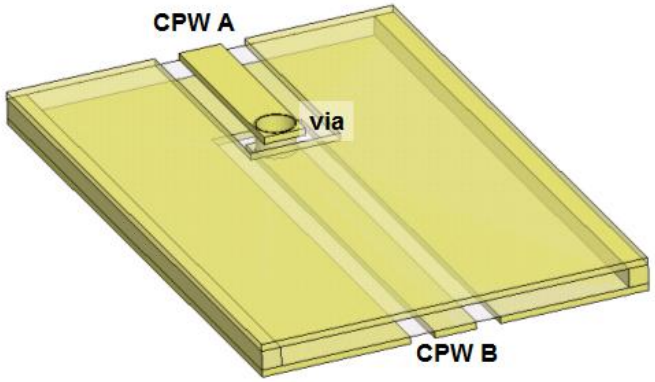


Figure 41: CPW line to CPW line through via interconnection.

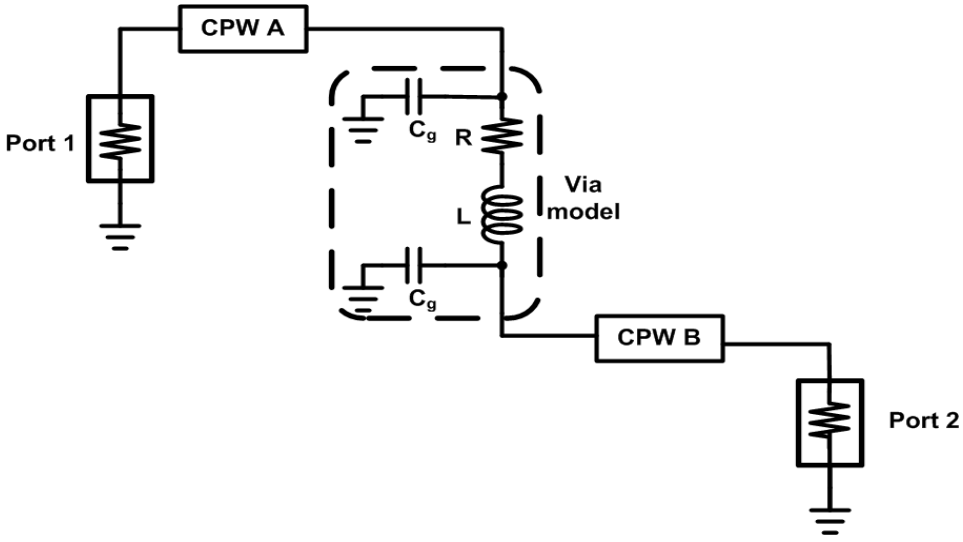


Figure 42: Schematic of the model simulation with the CPW lines.

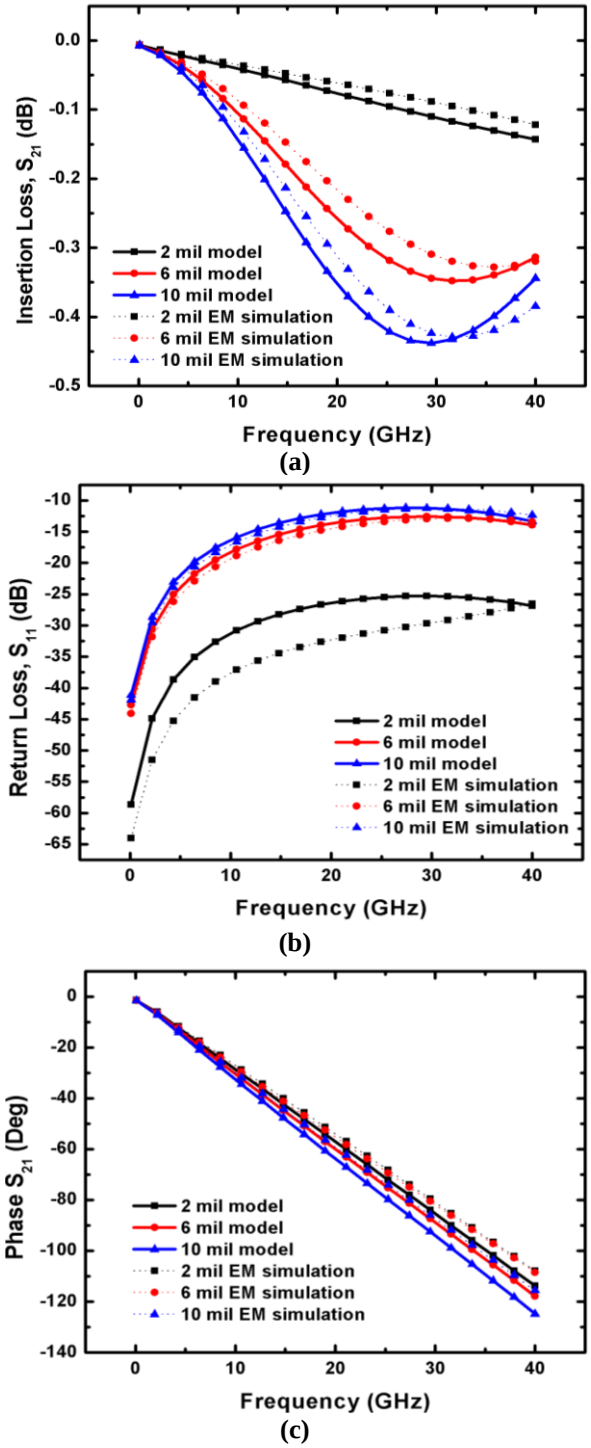


Figure 43: EM and Model simulations for 2, 6, and 10 mil via heights: (a) magnitude of S_{21} in dB, (b) magnitude of S_{11} in dB, and (c) phase of S_{21} in degree.

Through the comparisons in Figure 43, the via interconnect model gives a good agreement with EM simulation results. However, the model simulations take much shorter time to complete as compared with the EM simulations.

4.5 Verification of Simulation with Measurement using a PCB Multi-Layer Test Structure

Figure 44 shows the cross-section of a multi-layer printed circuit board with embedded capacitance layer. The dielectric constant of the capacitance layer is 26 (at 1 GHz) and the thickness is 16 microns. The cross-section view of the embedded capacitance layer sandwiched in between two 35 micron thick metal layers is shown in Figure 45.

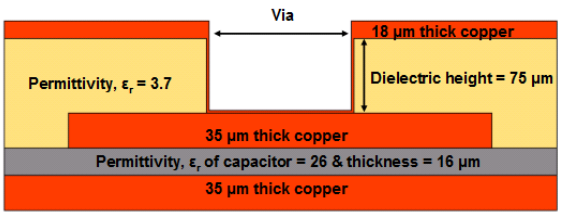


Figure 44: Cross-section of a multi-layer PCB board.

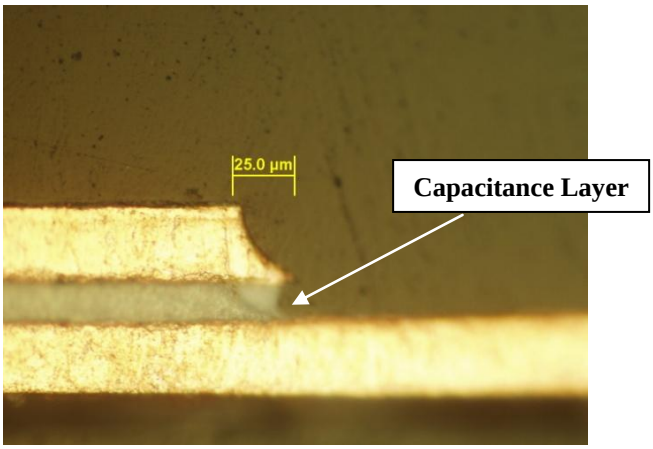


Figure 45: Cross-section view of the embedded 16 micron thick capacitance layer.

The top view of the board layout with different geometries and sizes of the capacitors at an internal layer is shown in Figure 46. Circular capacitor electrodes of five different diameters (C1 through C5) resulting in a capacitance of 1.42, 7.1, 14.2, 71, and 142 pF, were fabricated using the concept of distributed capacitance. Photomicrograph of the fabricated capacitors is shown in Figure 47. Details of the fabrication and S-parameter results are presented in [60].

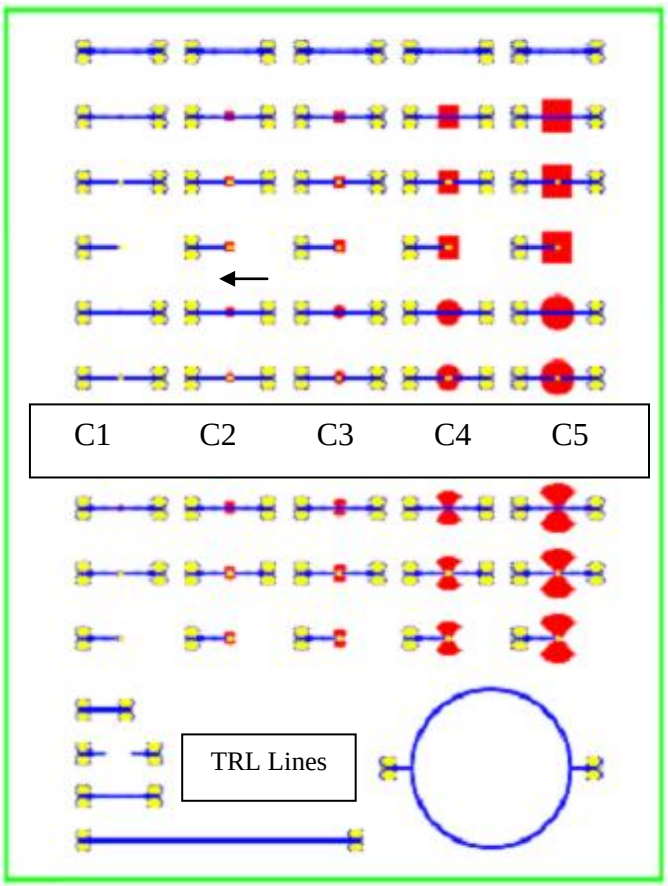


Figure 46: Top view of the multi-layer double-sided PCB board. The red circles in a row marked by the arrow represent five circular capacitors (C1 through C5) that are modeled and measured.

Figure 47: Photomicrograph of the fabricated circular capacitors C1 through C5.

The measured S-parameter data for the five circular capacitors are shown in Figure 48. After the parasitic model of the via was extracted, in the model simulation, the via resistance was assumed to be 0.1 Ω, the via inductance was assumed to be 5 pH, and the via capacitance due to the coupling between the via and the top metal of the capacitor was assumed to be 7 pF. The model simulation results are shown in Figure 49. The model simulations show good agreement with the measurement results.

4.6 Summary

The modeling results of via interconnections on organic substrates are presented. The S-parameter matrix which is extracted from EM simulation of a single via structure can be used to derive the equivalent electrical circuit model for the via interconnection. The lumped-element model can be used to replace the EM simulations, especially for circuits that have many via interconnection. This approach helps to reduce the complexity and time taken for the EM simulation. The model simulation results of the embedded capacitors match closely with the measured results.

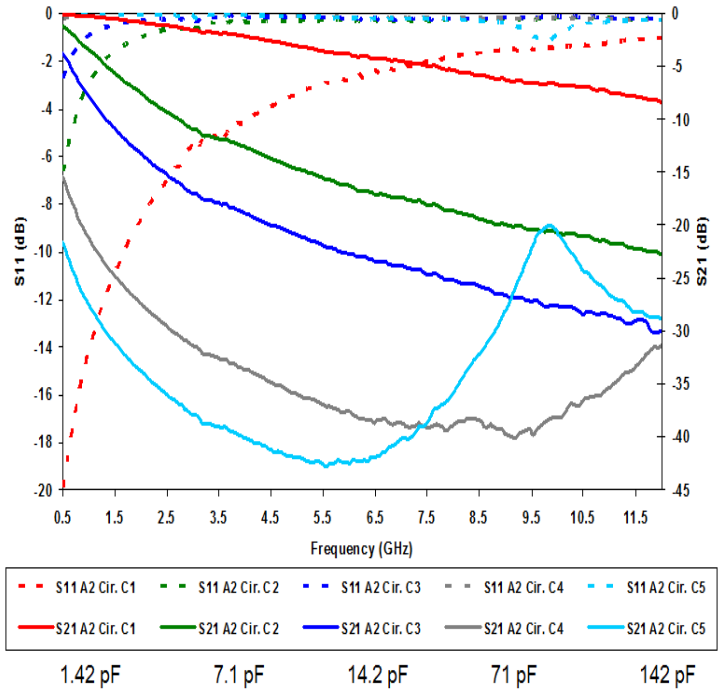


Figure 48: Measured S-parameter data of the embedded shunt capacitances [60].

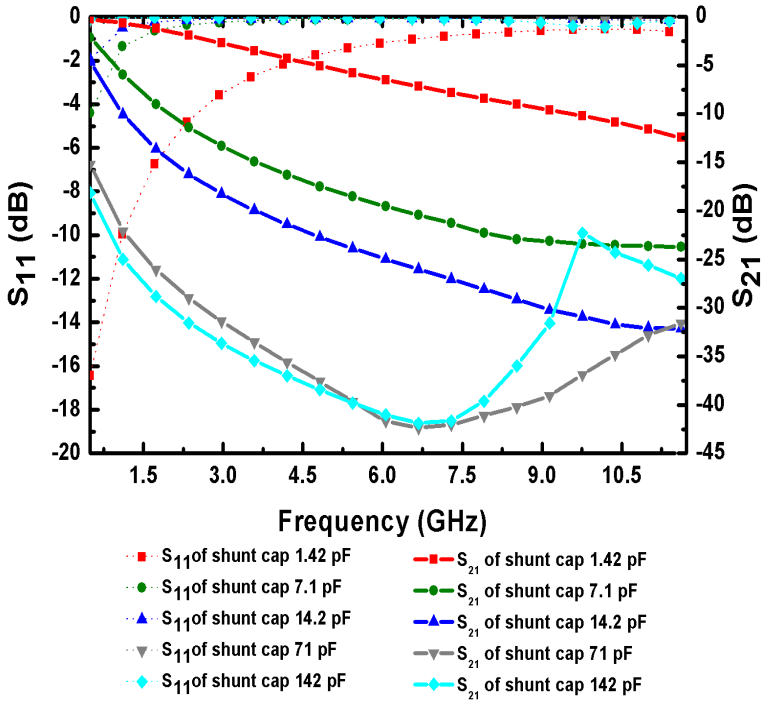


Figure 49: Model-simulated S-parameter results of the embedded shunt capacitances.

CHAPTER V

DE-EMBEDDING TRANSMISSION LINES USING A FULL-WAVE EM-SIMULATED PAD MODEL

5.1 Introduction

With increasing demand in functionality and performance in wireless devices, applications are increasingly moving towards SOC approaches. In SOCs, there are many different components integrated on a single chip and therefore, transmission lines play a very important role in determining the overall system performance. In addition, as device technologies continue to evolve, applications are pushing towards increasingly higher frequencies, wavelengths are getting smaller than the physical size of on-die components, and the transmission lines have to adopt particular geometries to ensure signal integrity.

Clearly, most RF/microwave test structures come with probing pads. As the frequency increases, the parasitics from the probing pads themselves will impact the performance of the transmission lines [61]. Hence, an accurate method to de-embed the pads in order to extract the data of the transmission line in question is required. Most pad de-embedding methods work well at low frequencies, but as the frequency increases, there are EM phenomena such as distributive effects, couplings of EM field lines, and skin effect, all of which make it difficult to accurately de-embed the pads. In this dissertation, EM simulations are used to model the probing pads since the EM software is able to capture most of the needed EM phenomena. Once the model is well-defined, using the ABCD matrices, the parameters of the transmission line can be easily extracted from the test structure. To validate the proposed de-embedding method, the de-embedded S-parameter results were compared with the results from the full EM simulation of a transmission line without the probing pads.

5.2 Pad De-Embedding Method

Figure 50 shows the photomicrograph of an on-chip microstrip line fabricated on a six-metal layer SiGe BiCMOS process (Jazz SBC-18). The transmission line is 500 μm in length, excluding the probing pads. The RF probes used for measuring the transmission lines were GGB Industries Model 67A GSG coplanar microwave probes. The calibration was performed with a probe-level short-open-load-thru (SOLT) standard on a GGB Industries CS-5 calibration substrate to account for any cable losses. The S-parameters of the transmission lines were measured using an Agilent E8361C VNA from 1 to 67 GHz. Measurements were performed on three separate dies to ensure consistency in the measured results.

The measured results, however, clearly do not reflect the actual performance of the transmission lines, as the probing pads contain parasitics, which could affect the transmission line performance, especially at high frequencies. Therefore, it is necessary to properly de-embed the pad parasitics from the measurement data.

There are many de-embedding methods. One of the most common techniques is the "open-short" approach [62], which is given as

$$Y_{dut} = \left[(Y_{measured} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1} \right]^{-1}, \tag{38}$$

where Y_{open} and Y_{short} are the two-port admittance parameters measured on a "open" test structure and a "short" test structure. The $Y_{measured}$ is the measured two-port admittance of the device and Y_{dut} is the de-embedded Y-parameters of the transmission line. Figure 51 shows the "open" and "short" test structures for de-embedding the pads.

Another common de-embedding technique is the symmetrical-line method [63], in which two transmission lines of different lengths are used, as shown in Figure 52. The shorter line is a "through" line while the longer line is the actual transmission line to be measured. Here, the through line is first measured to extract the ABCD matrix of the pad, as in (39). Then, using (40), the pads are de-embedded from the transmission line.

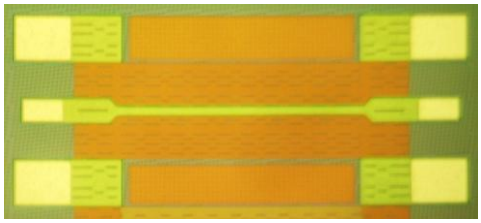


Figure 50: Photomicrograph of an on-chip microstrip.

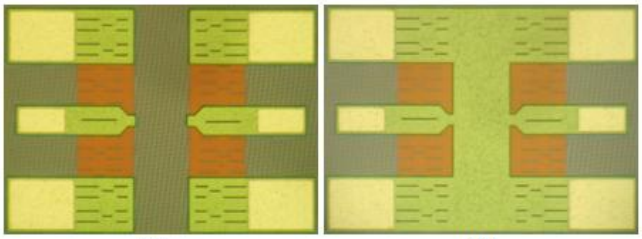


Figure 51: (a) "Open" test structure and (b) "short" test structure.

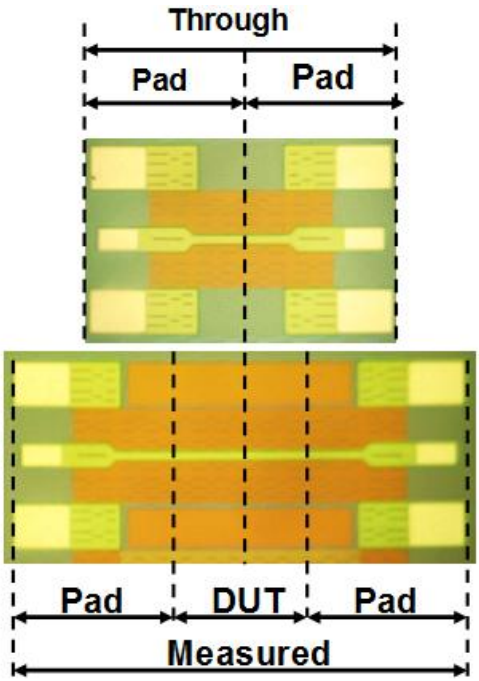


Figure 52: The symmetrical-line de-embedding method.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Pad} * \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Pad} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Through} \tag{39}$$

and

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{DUT} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Pad}^{-1} * \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Measured} * \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Pad}^{-1} \tag{40}$$

However, both of these methods have their disadvantages. The "open-short" method starts to lose it accuracy at higher frequencies, as the parasitics become more distributive [19]. For the symmetrical-line method, the S-parameter matrix of a single pad is always assumed to be symmetrical. However, in most cases, the S_{11} and S_{22} of a single pad are different, as in (41)

$$[S]_{11} \neq [S]_{22} \tag{41}$$

and hence in Figure 53,

$$[S]_{ii\_Left} \neq [S]_{ii\_Right} \tag{42}$$

where i = 1 or 2.

Therefore, the symmetrical-line approach is prone to error as the difference between the S_{11} and S_{22} of the single pad becomes larger.

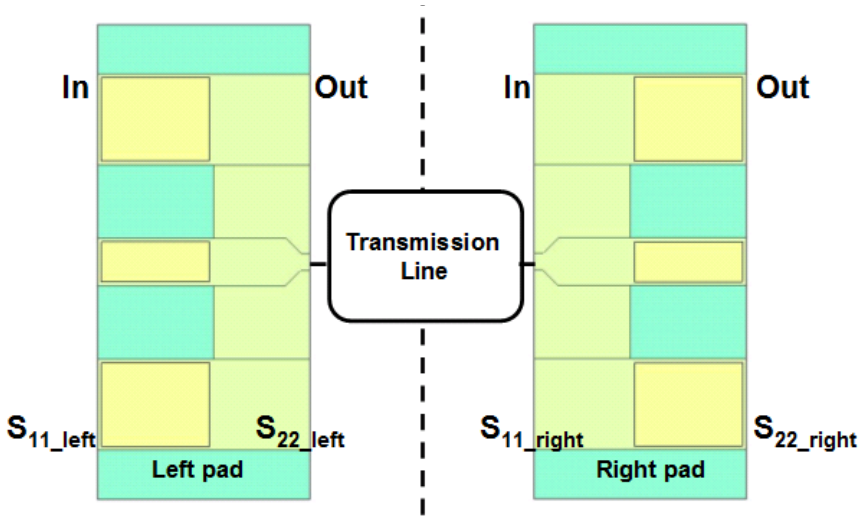


Figure 53: The left and the right pads of the transmission line test structures.

In this dissertation, commercially-available full-wave EM software was used to solve for the pad S-parameter matrices [64]. After which, the pads were then de-embedded from the measured data. Although running an EM simulation may be time consuming, it has proven to be a very reliable tool for extracting parasitic effect that could impact the circuit performance at high frequencies [65]. In the EM simulations used here, the dielectric constant of the oxide layer was varied to match the measured data. Figure 54 shows an EM-simulated structure of the on-chip microstrip line with bondpads. A comparison of S-parameter results between the EM simulated and measured data is shown in Figure 55.

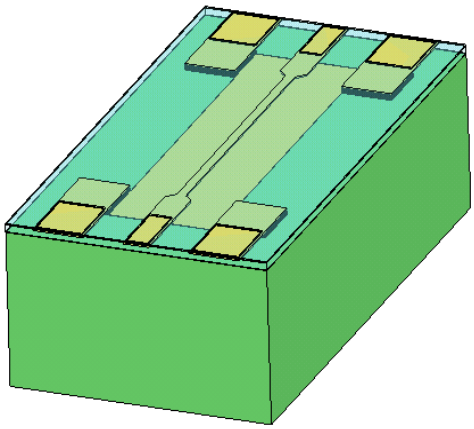


Figure 54: EM-simulated structure of the on-chip microstrip with pads.

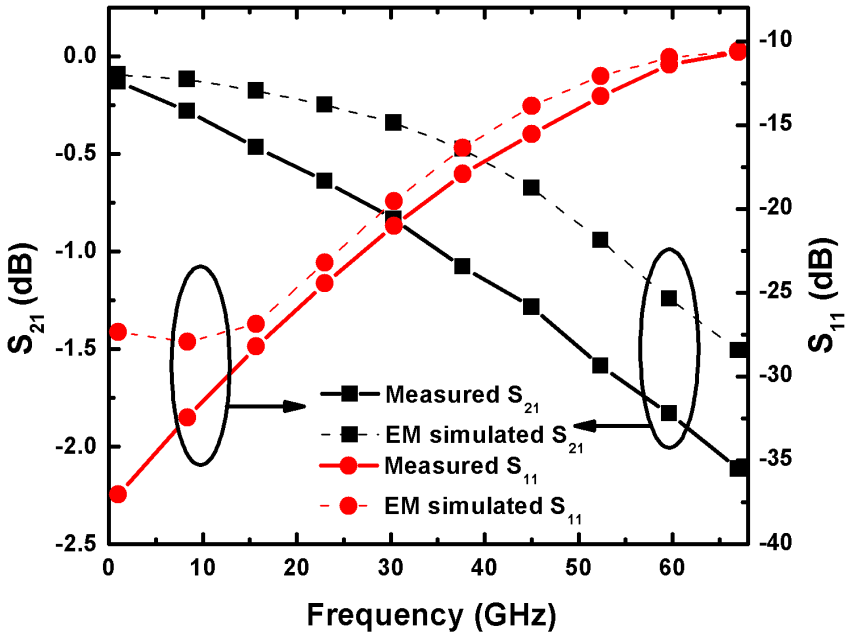


Figure 55: Comparison of S-parameter results between the EM-simulated and the measured data.

From Figure 55, it can be shown that the S-parameter results of the EM-simulated structure agree with the measured data. With the assumption that the EM model was accurate, an EM simulation was done on a single pad, as shown in Figure 56. In this case, the EM simulation was performed on the left probing pad.

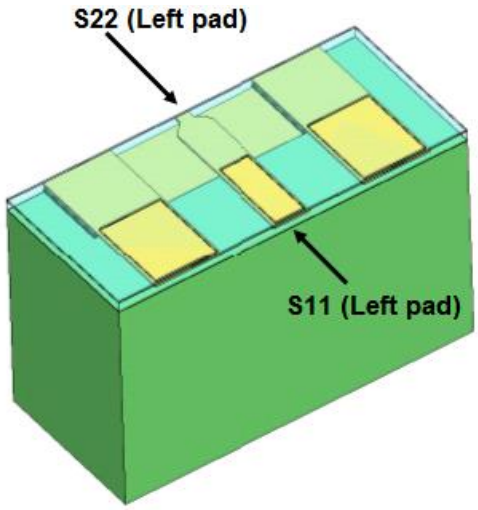


Figure 56: EM-simulated structure of the left probing pad.

As shown in Figure 57, the EM-simulated results show that the magnitudes of S_{11} and S_{22} have a difference of about 5 dB. Hence, using the symmetrical-line method will likely lead to significant errors.

The relationships between the left and right pad are expressed as follows:

$$S_{ij\_left} = S_{ji\_right} \tag{43}$$

and

$$S_{ii\_left} = S_{jj\_right}\ , \tag{44}$$

where $i, j = 1$ or 2, and $i \neq j$.

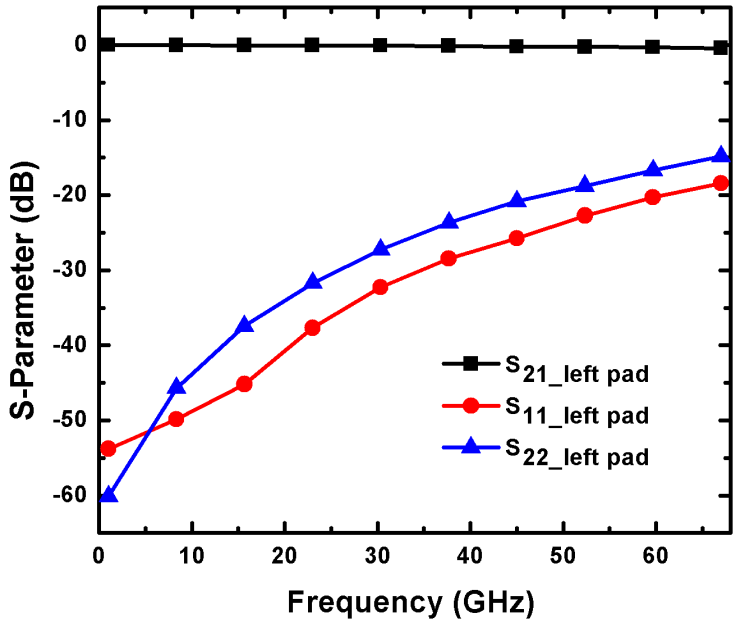


Figure 57: EM-simulated results of the left probing pad.

The S-parameter matrices for the pads are converted into ABCD matrices [66]. The relationship between the S-parameter matrix and ABCD matrix are as follows:

$$A = \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{2S_{21}}, \tag{45}$$

$$B = 50\frac{(1+S_{11})(1+S_{22})-S_{12}S_{21}}{2S_{21}}, \tag{46}$$

$$C = \frac{1}{50}\frac{(1-S_{11})(1-S_{22})-S_{12}S_{21}}{2S_{21}}, \tag{47}$$

and

$$D = \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{2S_{21}}. \tag{48}$$

The de-embedded transmission line is then given as,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{DUT} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}^{-1}_{Left\_pad} * \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Measured} * \begin{bmatrix} A & B \\ C & D \end{bmatrix}^{-1}_{Right\_pad}. \tag{49}$$

To verify the present method of EM-simulated-pad de-embedding, the on-chip microstrip was simulated in HFSS without its pads, as shown in Figure 58. Comparisons were made between the different de-embedding methods and the results are shown in Figure 59. In Figure 59, all of the de-embedding methods have the similar S-parameter response below 10 GHz. However, beyond 10 GHz, the open-short de-embedding method and the symmetrical-line de-embedding method begin to lose their accuracies. On the other hand, the S-parameter result which is extracted from the EM-simulated-pad de-embedding method is still able to maintain a close agreement with the EM-simulated S-parameters up to 67 GHz.

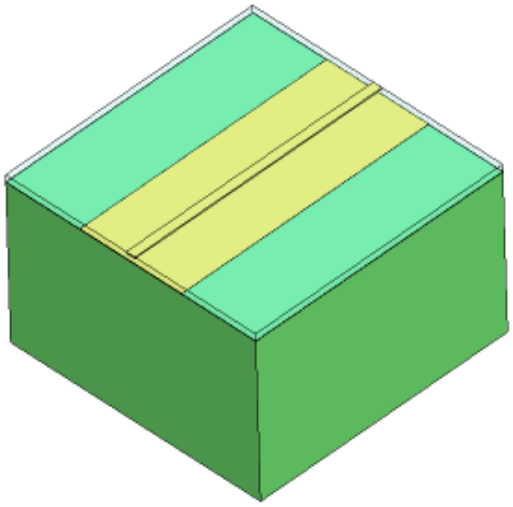
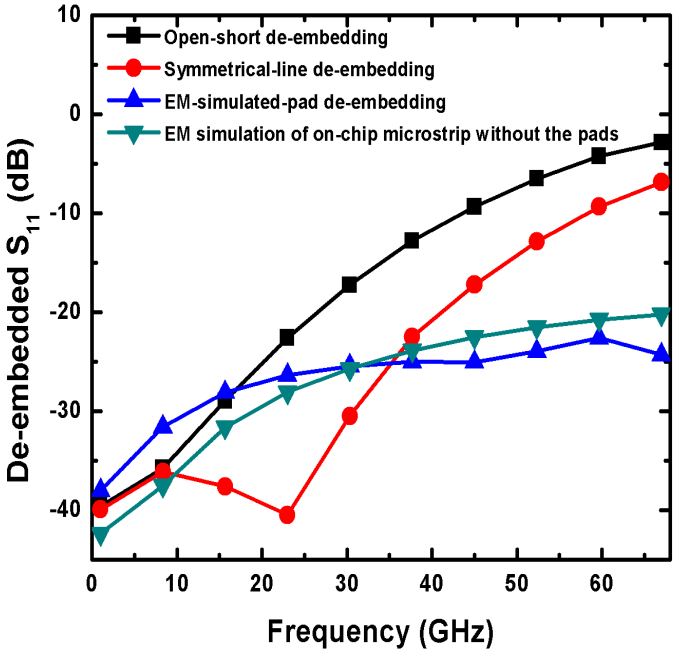
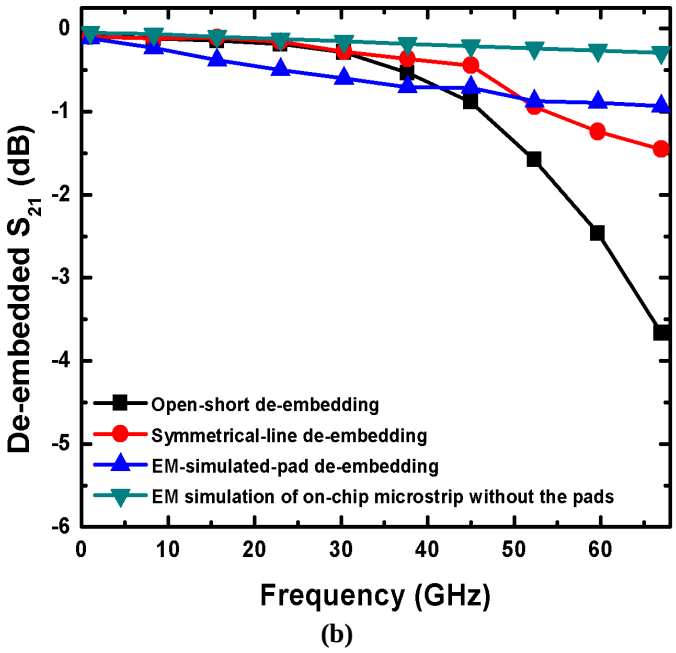


Figure 58: EM-simulated structure of the on-chip microstrip without the pads.



(a)



(b)

Figure 59: Comparison of the S-parameters by various de-embedding methods: (a) magnitude of S_{11} in dB and (b) magnitude of S_{21} in dB.

From the de-embedded ABCD matrix in (49), the propagation constant (γ) and the characteristic impedance (Z) of a lossy transmission line can be derived using (50) and (51) [66],

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{DUT} = \begin{bmatrix} \cosh \gamma l & Z \sinh \gamma l \\ \frac{1}{Z} \sinh \gamma l & \cos \gamma l \end{bmatrix}, \tag{50}$$

$$\gamma = \frac{\cosh^{-1}(A)}{l}, \tag{51}$$

and

$$Z = \frac{B}{\sinh \gamma l}, \tag{52}$$

where l is the physical length of the microstrip.

In the EM simulations, the characteristic impedance for the EM structure can be calculated with HFSS software using the wave-port excitation mode. The characteristic impedances for the various de-embedding methods were calculated via (52). In Figure 60, the characteristic impedances from different de-embedding methods were extracted and compared with the calculated characteristic impedance. It can be shown that the characteristic impedance from the EM-simulated-pad de-embedding method has the closest match with the calculated characteristic impedance.

Comparing the different approaches of de-embedding transmission lines, as shown in Figures 59 and 60, the EM-simulated-pad de-embedding technique gives the best match to data up to 67 GHz. Both the "open-short" and the symmetrical-line de-embedding methods begin to lose their accuracies at above 20 GHz. Therefore, the EM-simulated-pad de-embedding method appears to be more promising.

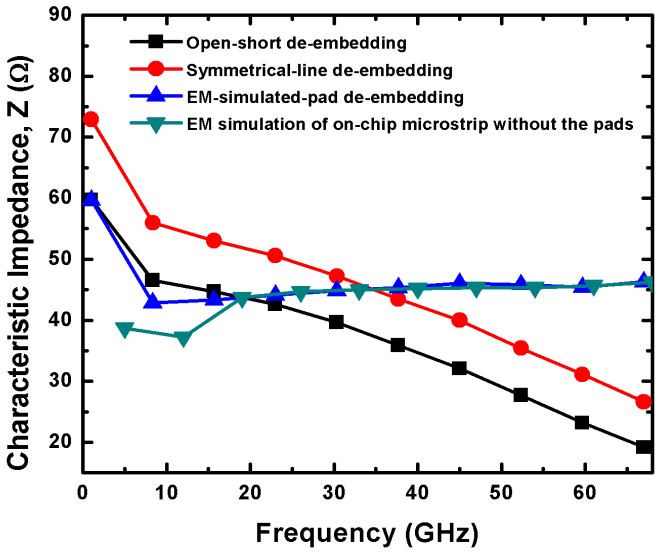


Figure 60: Comparison of characteristic impedances by various de-embedding methods.

5.3 Summary

A new method to de-embed the probing pads in test structures is presented. This method uses EM simulations to extract the pad parasitics. Using the EM models, the ABCD matrices of the pads can be de-embedded from the test structures to extract the measured data. Different de-embedding methods were used and compared with the EM simulated results. The EM-simulated-pad de-embedding method proved to be most accurate and shows good agreement up to 67 GHz.

CHAPTER VI

LOW-POWER AND LOW-VOLTAGE X-BAND SIGE HBT LOW-NOISE AMPLIFIER

6.1 Introduction

Low-power consumption is one of the main drivers for many defense and commercial wireless applications. Every wireless communication system consists of a signal transmitter and a signal receiver. The LNA is a key component of the receiver. Its role is to amplify the incoming signal while minimizing distortion and added noise. Since most receivers are hand-held or battery-operated devices, power consumption is a key factor to consider when designing an LNA. In addition, low power operation must be achieved without compromising gain or noise figure.

The cascode configuration has been a popular topology for designing high performance LNAs [67,68,69]. The cascode structure reduces the unwanted Miller-capacitance effects. However, since two transistors are stacked on top of each other, the cascode topology requires a higher supply voltage (> 1.0 V), which makes it unsuitable for low-voltage applications [70].

For applications requiring very low supply voltages, the common-emitter (CE) topology is typically utilized. Ultra-low-power LNAs [71,72,73,74,75] that use less than 2 mW of *dc* power have been recently reported. However, these LNAs usually suffer from high *NF* (> 3.5 dB) and operate at lower frequencies (< 5.5 GHz). Decreasing power and increasing operating frequency tend to degrade both the noise and gain performance. Thus, the design of a low-power X-band LNA is very challenging. Recently, it has been shown that a weakly saturated SiGe HBT can enable low-voltage RF front-end design [76]. An X-band LNA design based on this intentional saturation principle has been presented [77]. Although the LNA supply voltage was as low as 1.0 V, its *dc* power consumption was still more than 2 mW.

The present work investigates the design of an X-band LNA using a 200 nm, 150 GHz peak f_T SiGe HBT BiCMOS process technology (Jazz SBC-18). The LNA is optimized for low-supply voltage (< 1.0 V) and low-power consumption (< 2 mW), at 10 GHz. For the first time, the SiGe LNA is biased in both the forward-active (FA) and weak-saturation (WS) modes and compared on their principal figures-of-merits (FOMs) in a head-to-head fashion. The measured results show that by driving the SiGe LNA in the WS mode, the *dc* power consumption of the LNA can be reduced without any major deterioration of the gain and noise performance. Given the same power consumption, the SiGe LNA in WS mode has a higher gain and a higher input-referred 1-dB compression point (P_{1dB}) than in the FA mode. In WS mode, when the collector voltage (V_{cc}) and collector current (I_c) are set at 0.5 V and 1 mA, respectively, the SiGe LNA achieves a gain of more than 8.5 dB and *NF* of 3.1 dB at 10 GHz. This yields a gain per *dc* power consumption FOM of 17 dB/mW. To the best of our knowledge, this is by far the highest reported to date for X-band SiGe LNAs.

6.2 Circuit Design

6.2.1 Noise Analysis

The proposed low-power SiGe HBT LNA uses a CE configuration that offers the best compromise between the *NF* and the power gain[19]. The noise factor (*F*) of a two-port network is expressed as a function of the source admittance (Y_s) and the noise parameters [78]-[79]

$$F = F_{\min} + \frac{R_n}{G_s}\left|Y_s - Y_{opt}\right|^2, \tag{53}$$

where G_s is the real part of Y_s, $F_{\min}$ is the minimum noise factor, R_n is the noise resistance, and Y_{opt} is the optimum admittance of the system. The *NF* is related to *F* through the following expression,

$$NF = 10 \log F \, . \tag{54}$$

The small-signal noise model of a SiGe HBT is shown in Figure 61, where r_b is the base resistance, r_π is the base-emitter resistance, C_{be} is the base-emitter junction capacitance, and C_{bc} is the base-collector junction capacitance. The $\overline{i_b^2}$ and $\overline{i_c^2}$ are the base and collector mean-square shot noise current sources in the frequency band Δf,

$$\overline{i_b^2} = 2qI_b \Delta f \, , \tag{55}$$

$$\overline{i_c^2} = 2qI_c \Delta f \, , \tag{56}$$

where q is the electronic charge (1.60 x 10^{-19} C), I_b is the base current, and I_c is the collector current. The $\overline{v_b^2}$ is the mean-square thermal noise source produced by the r_b,

$$\overline{v_b^2} = 4kTr_b \Delta f \, , \tag{57}$$

where k is Boltzmann's constant (1.38 x 10^{-38} J/K), and T is the absolute temperature in Kelvins.

From Figure 61, an expression for F_{min} in (53) can be derived as follows [20]:

$$F_{min} = 1 + \frac{1}{\beta} + \sqrt{2g_m r_b} \sqrt{\frac{1}{\beta} + \left(\frac{f}{f_T} \right)^2} \, , \tag{58}$$

where $\beta = I_c / I_b$, $g_m = qI_c / kT$, and f_T is the unity-gain cutoff frequency in the SiGe HBT.

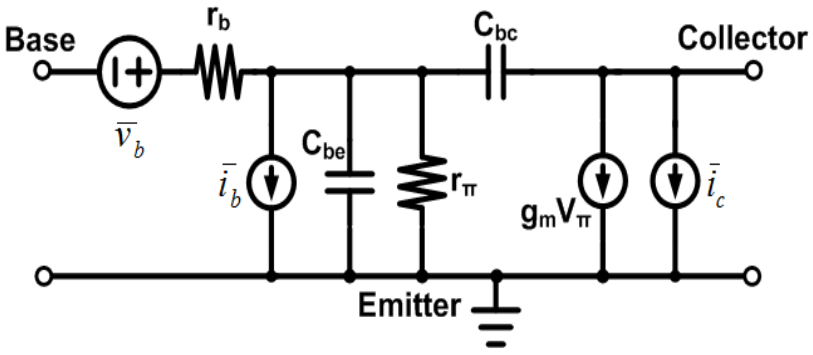


Figure 61: Small-signal noise model of a SiGe HBT.

Through (58), it can be shown that the F_{min} increases (degrades) with frequency (f). In addition, devices with higher β, lower r_b, and higher f_T are preferred for low-noise applications.

Assuming that the transistor is biased at a fixed collector current density (J_c), when the emitter stripe width (W_e) increases by a scaling factor of M, both g_m and r_b of the transistor are multiplied by M. From (58), the F_{min} can be re-expressed to include the scaling factor as

$$F_{min} = 1 + \frac{1}{\beta} + M\sqrt{2g_m r_b}\sqrt{\frac{1}{\beta} + \left(\frac{f}{f_T}\right)^2} \,. \tag{59}$$

According to (59), at a fixed J_c, a small W_e should be used to improve the F_{min}. On the other hand, when the emitter length (L_e) increases by a scaling factor N, g_m is multiplied by N, while r_b is divided by N. As a result, the scaling effect of N cancels out through (58). Thus, for a fixed J_c, L_e has very little effect on the F_{min}.

6.2.2 Device Size Selection for Low-Power Considerations

To achieve a low F_{min}, the present design uses the minimum allowable W_e of 0.2 μm. In this case, I_c is fixed at 1 mA, with V_{cc} set at 1 V, so that the maximum *dc* power consumption (P_{dc}) of the LNA is kept at 1 mW. Both the available gain (G_A) and minimum noise figure (NF_{min}) are functions of J_c. The J_c of the SiGe HBT is given as

$$J_c = \frac{I_c}{L_e W_e} \,. \tag{60}$$

Since I_c and W_e in (60) are kept constant, L_e is scaled such that the device can operate at a J_c that effectively balances gain and noise performance for the LNA. The G_A is the operating gain with conjugate matches at the amplifier input and output, and is expressed as

$$G_A = \frac{|S_{21}|^2 (1-|\Gamma_{in}|)^2}{|1-S_{11}\Gamma_{in}^*|^2 (1-|\Gamma_{out}|^2)}, \tag{61}$$

where Γ_{in} and Γ_{out} are the input and output reflection coefficients, respectively. Figure 62 shows the simulations of G_A and NF_{min} as a function of L_e at 10 GHz, with P_{dc} = 1 mW.

For an LNA to achieve simultaneous noise and input power matching, the conjugate of its input impedance (Z_{in}*) has to be equal to the optimum source impedance (Z_{opt}) [80]. The Z_{in} can be calculated from the S-parameters and is given as,

$$Z_{in} = 50\frac{1+S_{11}}{1-S_{11}}, \tag{62}$$

and the Z_{opt} is given as,

$$Z_{opt} = \frac{1}{Y_{opt}}. \tag{63}$$

The real terms of Z_{in}* and Z_{opt} can be expressed as follows [20]:

$$Real\ Z_{in}^* = \frac{\beta}{g_m} + r_b, \tag{64}$$

and

$$Real\ Z_{opt} = \frac{f_T}{f}\frac{1}{\sqrt{L_e}}\sqrt{\frac{2r_b}{J_c W_e}\frac{kT}{q}}. \tag{65}$$

Analyzing (64) and (65) reveals that by increasing L_e, both real terms of Z_{opt} and Z_{in}* decrease. Figure 63 shows the value of the *Real* Z_{opt} is brought closer to the *Real* Z_{in}* as L_e increases. The imaginary term of Z_{in}* (*Imag* Z_{in}*) maintains a good match with the imaginary term of Z_{opt} (*Imag* Z_{opt}) for all values of L_e.

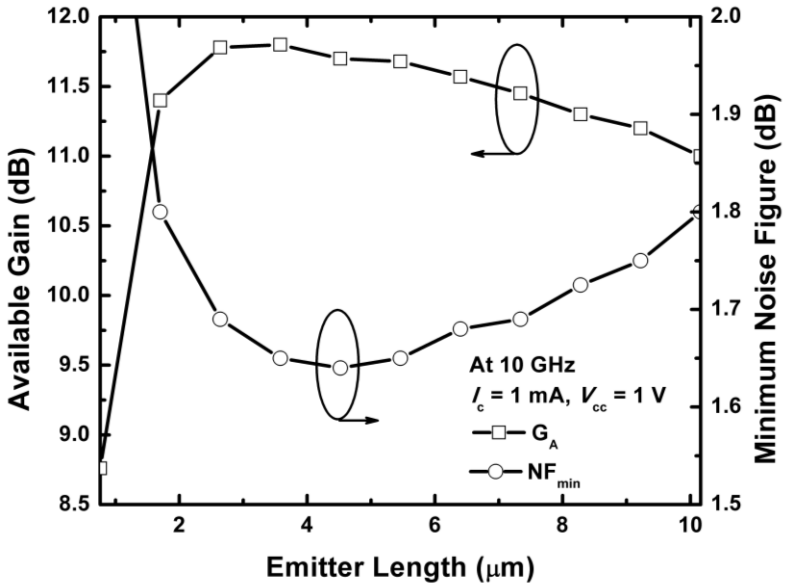


Figure 62: Simulations of G_A and NF_{min} as a function of L_e at 10 GHz.

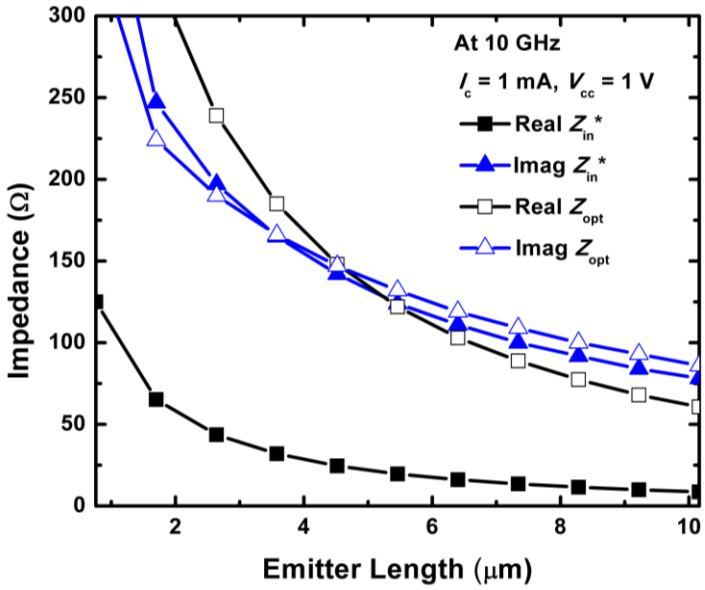


Figure 63: Simulations of the S_{11} and Z_{opt} as a function of L_e at 10 GHz.

For the LNA, the L_e of the SiGe HBT was selected to be 7.4 μm in length. At this length, the G_A is about 11.45 dB and the NF_{min} is about 1.7 dB, at 10 GHz. The Z_{in}* is about 13.55 + j100 Ω and the Z_{opt} is about 88.87 + j109 Ω. A source impedance (Z_{source}) for the LNA is selected approximately in between the Z_{in}* and Z_{opt} at 38.29 + j101.11 Ω.

This achieves a good trade-off between the gain and noise performance, as seen in Figure 64a. In the ideal simulations (without any parasitic loss) at 10 GHz, the simulated S_{21} and *NF* of the SiGe LNA are about 10.5 dB and 2.1 dB, respectively, with the load impedance (Z_{load}) of 51.23 - j23.67 Ω.

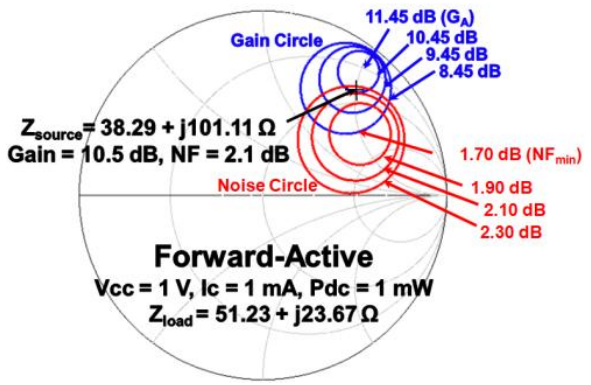
6.2.3 Weak-Saturation Mode

When the SiGe HBT in the LNA is biased in the WS region, the emitter-base and collector-base junctions are forward-biased, such that

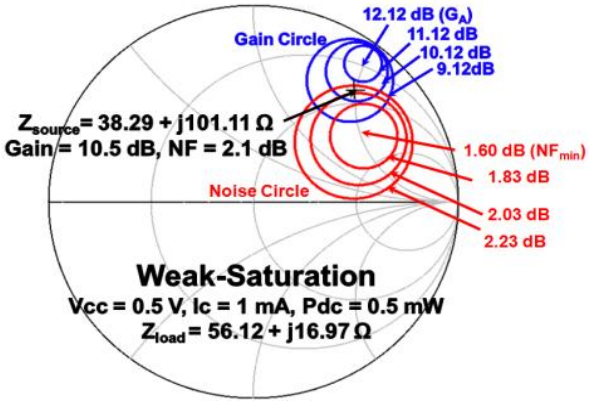
$$V_{ee} < V_b > V_{cc}, \tag{66}$$

where V_{ee} and V_b are the emitter voltage and the base voltage, respectively. Figure 64 shows the gain and noise circles at 10 GHz on Smith charts for the SiGe LNA biased in the FA mode (V_{cc} = 1 V) and the WS mode (V_{cc} = 0.5 V), with I_c = 1 mA. By keeping the J_c constant, the Z_{in}* and Z_{opt} of the LNA remains nearly unchanged.

As shown in Figure 64b, in the WS mode, the LNA has a simulated S_{21} and a *NF* of about 10.5 dB and 2.1 dB, respectively, when Z_{source} = 38.29 + j101.11 Ω and Z_{load} = 56.12 - j16.97 Ω. However, between the FA and WS modes, only one Z_{load} can be chosen, and in this case, the Z_{load} of the LNA is selected to be 51.23 - j23.67 Ω. It is expected that the gain and the NF_{min} of the WS LNA will degrade slightly as a result. However, in the WS mode, the SiGe LNA can benefit from operating with a much lower P_{dc}, presenting a favorable trade.



(a)



(b)

Figure 64: Gain and noise circles on the Smith Charts: (a) FA mode and (b) WS mode.

6.3 Measurement Results

6.3.1 Transmission Line Test Structures

In an RFIC, many different components are integrated on a single chip and therefore interconnections such as the transmission lines have a significant impact on the overall circuit performance. Test structures for 50 Ω transmission lines were fabricated and measured to compare the resultant RF performance. Two types of transmission lines were used for the test structures, namely the microstrip (MS) line and the co-planar waveguide (CPW) line. Each transmission line has a length of 500 μm excluding the

probing pads. Figure 65 shows the test structures for the transmission lines. The transmission lines were implemented in the Jazz SBC-18 process with six metal layers [81,82,83]. The M6 and M5 metal layers are used for the signal lines, while the M1 metal layer is used for the ground plane. Table 10 shows the physical dimensions for each transmission line.

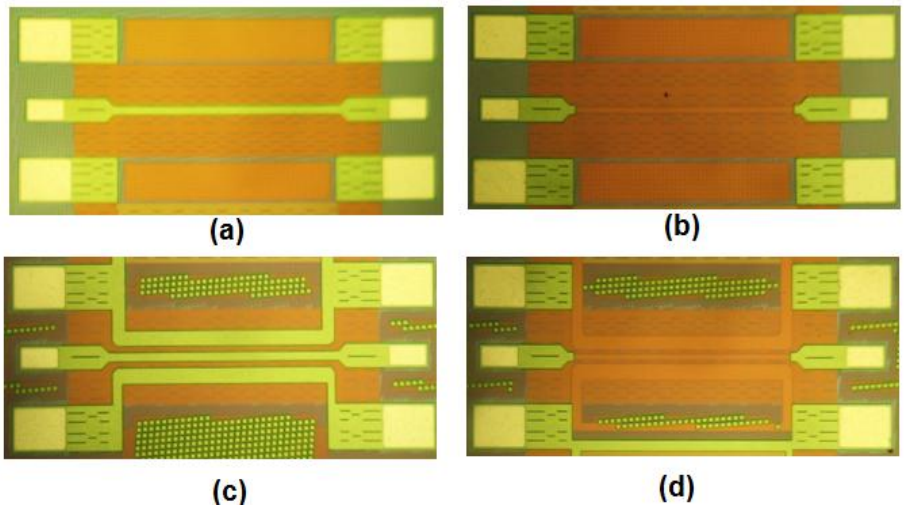


Figure 65: Transmission line test structures: (a) MS1, (b) MS2, (c) CPW1, and (d) CPW2.

Table 10: List of transmission lines.

Transmission line	Top layer	Bottom layer	W^{+} (µm)	G^{++} (µm)
MS1	M6	M1	17.3	-
MS2	M5	M1	11.0	-
CPW1	M6	M1	17.3	15.5
CPW2	M5	M1	11.0	9.8

$^{+}$ The width of the signal line.
$^{++}$ The spacing between the signal line and the ground plane in the CPW line.

Measurements were performed with an Agilent E8363B VNA from 5 to 20 GHz using GSG coplanar microwave probes of 150 μm wide pitch. The VNA was calibrated using a thru-reflect-line (TRL) standard. Figure 66 shows the measured S-parameter results for the transmission lines. As shown in Figure 66, all of the transmission lines have an insertion loss less than 0.7 dB and return loss of more than 20 dB, from 5 to 20 GHz. Signal lines using M6 metal layer have less insertion loss and better impedance match, as compared to those using M5 metal layer.

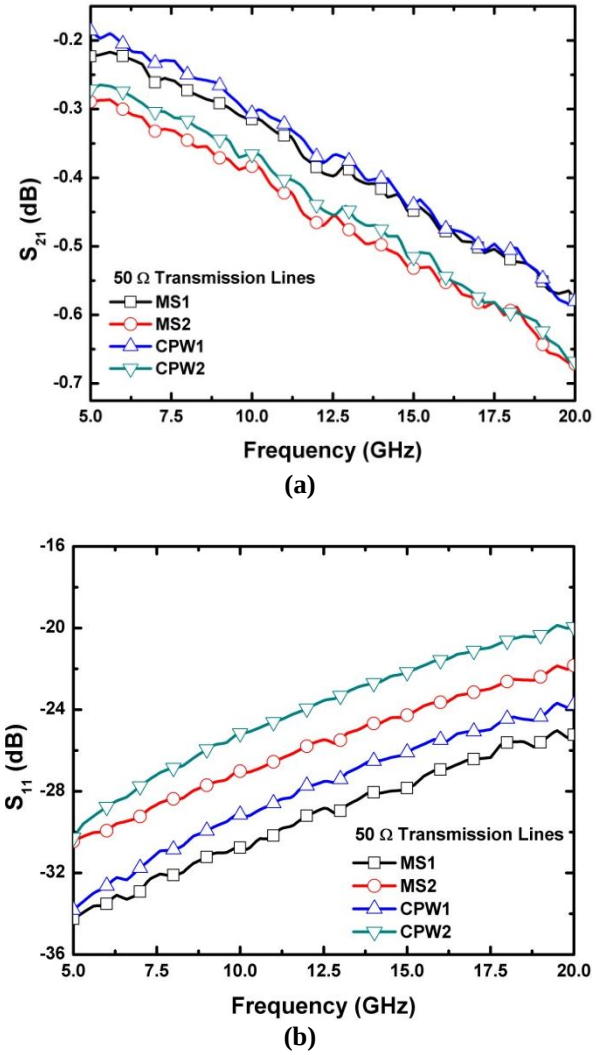


Figure 66: Measured S-parameters for the transmission lines: (a) magnitude of S_{21} in dB and (b) magnitude of S_{11} in dB.

At 10 GHz, MS1 and CPW1 have very similar insertion losses of 0.31 dB and 0.30 dB respectively. However, the return loss of MS1 is 1.7 dB higher than the return loss of CPW1. Based on these results, the transmission lines implemented in the SiGe LNA followed the MS1 design to achieve a better impedance match.

6.3.2 SiGe HBT LNA Operating under Forward-Active

Figure 67 shows the simplified schematic of the SiGe LNA. In the matching networks, the capacitances C_b (272 fF) and C_c (232 fF) act as *dc* blocks, the inductances L_b (1 nH) and L_c (1 nH) act as RF chokes, and the resistance R_c (250 Ω) stabilizes the LNA. The TL_1 (80 μm) and TL_2 (190 μm) are 50 Ω transmission lines, which are placed at the input and output of the SiGe LNA to minimize any potential loss in the RF signal due to impedance mismatch. Figure 68 shows the photomicrograph of the fabricated LNA die. The total die area including the bond pads is 0.75 x 0.75 mm^2.

Figure 69 shows the measured and post-extraction simulated S-parameters of the SiGe LNA, where the V_{cc} = 1.0 V and I_c = 1.0 mA, yielding a total power dissipation of 1.0 mW. In this case, the SiGe HBT is biased in the FA mode. The measurement was performed on-wafer using GSG coplanar microwave probes, with a TRL probe-level calibration to account for the cable losses. In Figure 69, the measured results show that the SiGe LNA has a gain of 9.0 dB at 10 GHz, and peak gain of 10 dB at 9 GHz. At 10 GHz, the input return loss, the output return loss, and the isolation, are 5.05 dB, 13.5 dB, and 25.5 dB, respectively. The LNA has a good output impedance match from 8.4 to 11.4 GHz, where the S_{22} is less than -10 dB. On the input side, the S_{11} has been compromised for the noise matching. The S_{11} ranges from -14.5 to -5.0 dB between 8.0 and 10.1 GHz.

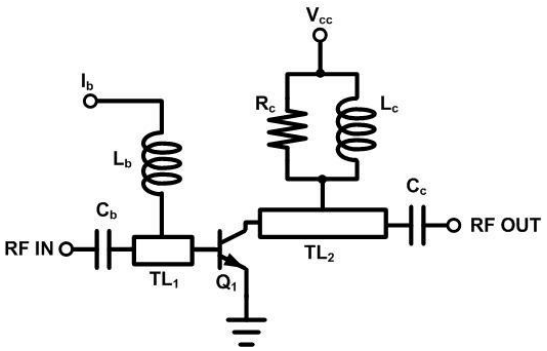


Figure 67: Schematic of the SiGe HBT LNA.

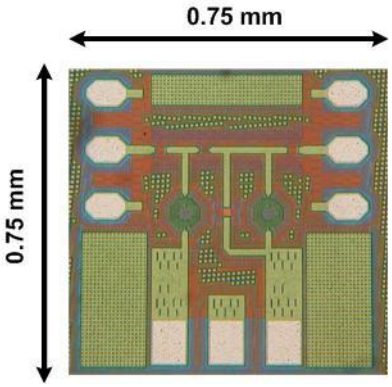


Figure 68: Photomicrograph of the SiGe HBT LNA.

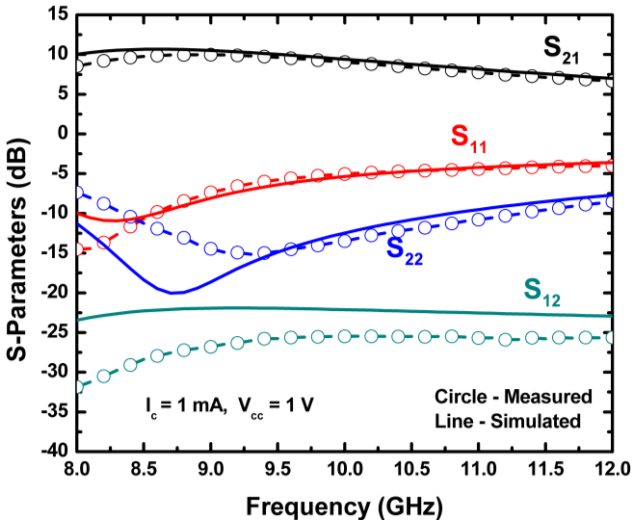
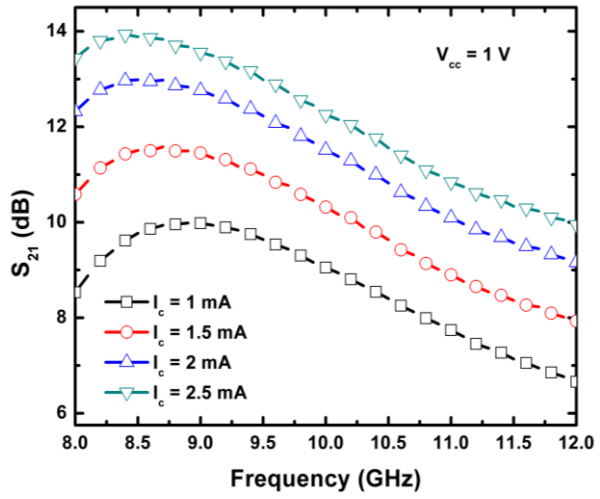
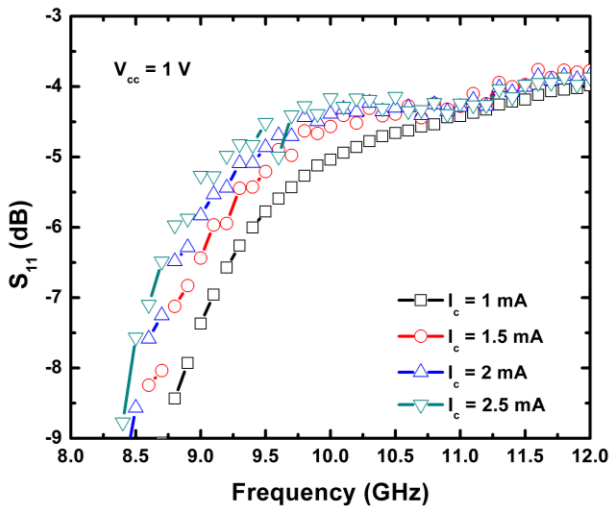


Figure 69: Simulated and measured S-parameter results of the SiGe LNA biasing at 1 mW in FA mode.

Increasing P_{dc} from 1 to 2.5 mW improves the S_{21} of the SiGe LNA. By increasing I_c from 1 to 2.5 mA, with V_{cc} kept constant at 1 V, the S_{21} improves by 3.2 dB (9.05 to 12.25 dB) at 10 GHz. Figure 70 shows how the measured S-parameters change with an increase in P_{dc}. Changing the J_c varies the input and output impedances of the SiGe LNA, which affects the impedance match. At 10 GHz, the S_{11} degrades slightly from -5.05 to -4.16 dB, while the S_{22} degrades from -13.5 to -11.4 dB.



(a)



(b)

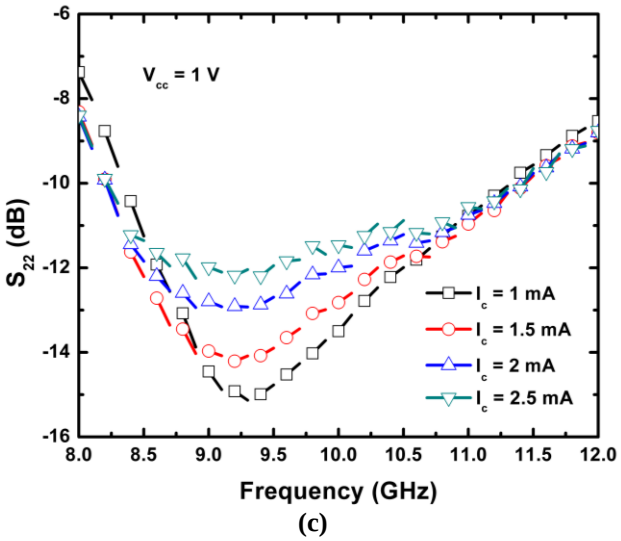


Figure 70: Measured S-Parameters of the SiGe LNA with I_c sweeping from 1.0 to 2.5 mA: (a) Magnitude of S_{21} in dB, (b) magnitude of S_{11} in dB, and (c) magnitude of S_{22} in dB.

6.3.3 SiGe HBT LNA Operating under Weak-Saturation

Decreasing V_{cc} and I_c helps to minimize the LNA *dc* power consumption, since

$$P_{dc} = V_{cc} I_c + V_b I_b \approx V_{cc} I_c , \tag{67}$$

where

$$V_{cc} I_c >> V_b I_b . \tag{68}$$

As the V_{cc} gets lower than V_b, the SiGe HBT begins to operate in the saturation region. Figure 71 shows the measured S_{21} of the SiGe LNA as the V_{cc} decreases from 1.0 V to 0.2 V, with I_c fixed at 1 mA.

When the SiGe HBT is biased in the hard-saturation (HS) region (V_{cc} < 0.3 V), the SiGe LNA gain begins to decrease drastically. Practically, there is a minimum V_{cc} to bias the SiGe LNA so that it can provide a sufficient gain. In Figure 71, when the SiGe HBT in the LNA is biased at V_{cc} = 0.5 V in the WS mode, the LNA is still able to supply more than 8.5 dB of gain at 10 GHz. In comparison to the FA mode, P_{dc} is reduced in half and the gain is decreased by only 0.55 dB.

To understand the effects of driving the SiGe HBT in saturation, multiple bias conditions were investigated. Table 11 shows a list of different bias conditions for the SiGe LNA. To ensure valid comparisons, the same SiGe LNA die was used throughout the S-parameter measurements.

Figure 72 shows the simulated output characteristics of the SiGe HBT. The regions where the LNA is biased are indicated on the plot. At 0.5 V, the SiGe HBT falls in the WS region. It is not recommended to bias the SiGe HBT below 0.5 V because there is a chance that with process variation, the SiGe HBT might fall into the HS region. As shown in Figure 71, the LNA loses significant gain when operating in the HS mode.

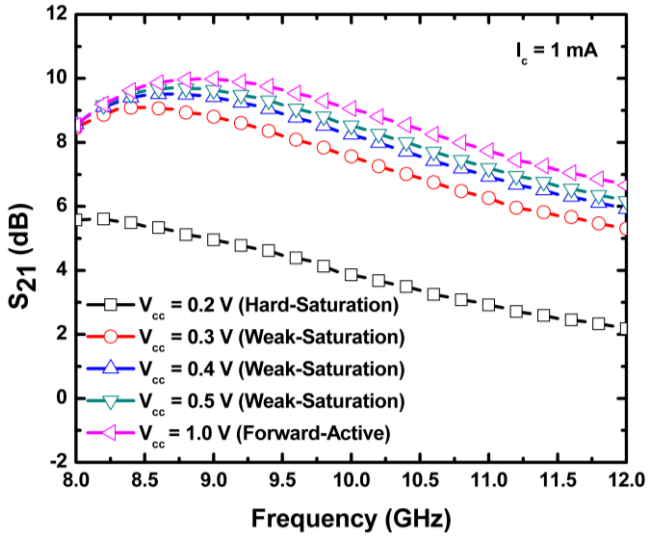


Figure 71: Measured S_{21} of the SiGe LNA for different values of V_{cc}.

Table 11: Bias conditions of the SiGe LNA.

Mode	V_{cc} (V)	I_c (mA)	P_{dc} (mW)
Weak-Saturation	0.5	1.0	0.5
Weak-Saturation	0.5	2.0	1.0
Forward-Active	1.0	1.0	1.0

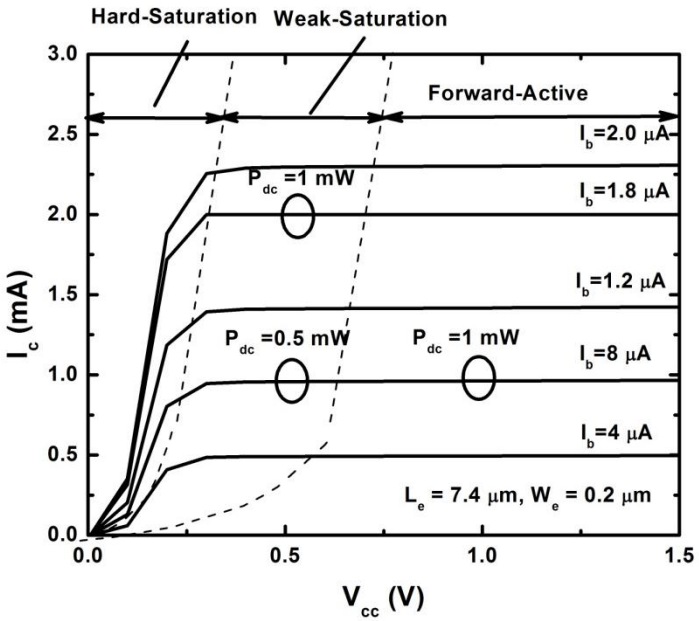


Figure 72: Output characteristics of the SiGe HBT.

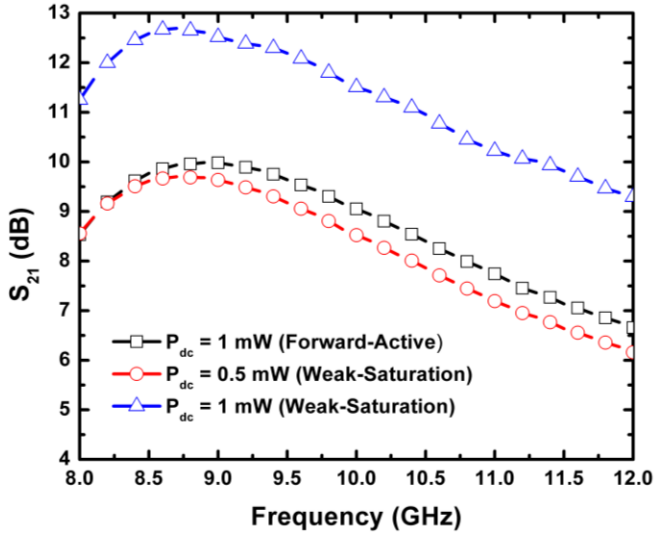
Table 12 summarizes the gain performance of the LNA for different bias conditions. Figure 73 shows the measured S-parameters for the SiGe LNA for different bias conditions.

As shown in Table 12, given the same P_{dc} = 1 mW, the S_{21} of the SiGe LNA in WS mode is 2.5 dB higher than in the FA mode. Therefore, biasing the SiGe HBT in the WS mode helps to improve the gain while consuming the same amount of *dc* power.

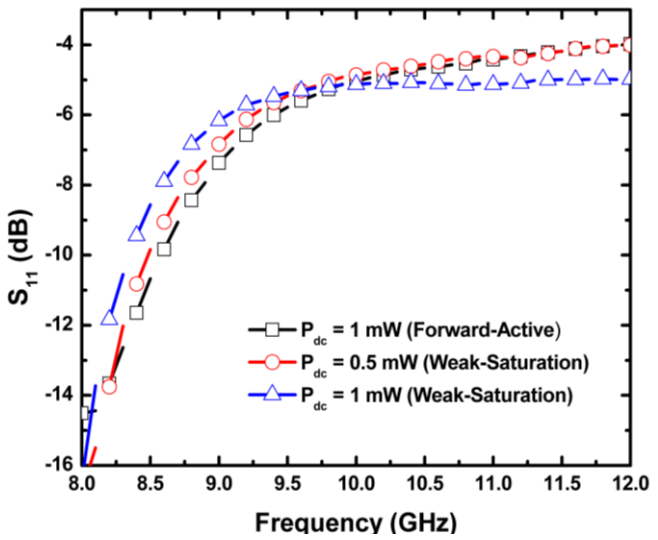
Figure 73b shows the measured S_{11} for different bias conditions. At 10 GHz, there is no major degradation in the measured S_{11} results. In the WS mode, the measured S_{11} at 10 GHz is -5.0 dB and -5.1 dB, where P_{dc} is at 0.5 mW and 1 mW, respectively. At the LNA output, the return loss degrades slightly when the LNA is biased in the WS mode. As shown in Figure 73c, the measured S_{22} at 10 GHz, is -11.6 dB and -10.2 dB, when P_{dc} is at 0.5 mW and 1 mW, respectively. Figure 73d shows that the SiGe LNA has more than 23 dB of isolation across X-band. The worst-case isolation occurs when the SiGe LNA is operating in the 0.5 mW WS mode and the measured S_{12} is about -23.7 dB at 10 GHz.

Table 12: Gain performance of the SiGe LNA for different bias conditions.

Mode	S_{21} at 10 GHz (dB)	Peak S_{21} (dB)
Weak-Saturation (0.5 mW)	8.5	9.7 (at 8.7 GHz)
Weak-Saturation (1 mW)	11.5	12.7 (at 8.7 GHz)
Forward-Active (1 mW)	9.0	10 (at 9 GHz)



(a)



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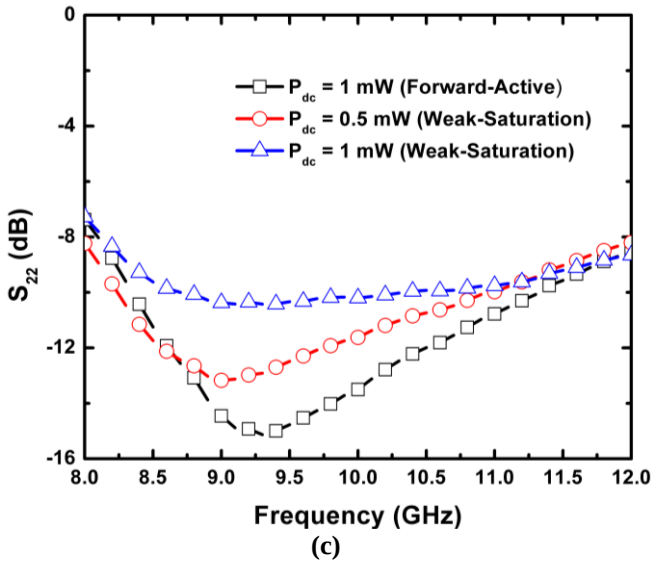

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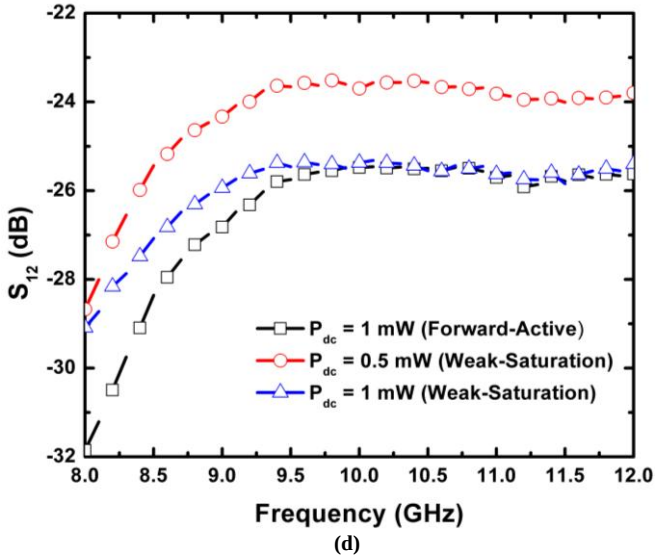


(d)

Figure 73: Measured S-Parameters of the SiGe LNA at different bias conditions: (a) magnitude of S_{21} in dB, (b) magnitude of S_{11} in dB, (c) magnitude of S_{22} in dB, and (d) magnitude of S_{12} in dB.

6.3.4 Noise Measurement

The *NF* was measured using the noise figure measurement personality in an Agilent E4446A Spectrum Analyzer. Figure 74 shows the simulated NF_{min}, simulated *NF*, and measured *NF* when the LNA is biased in the FA mode at I_c = 1 mA and V_{cc} = 1V. At 10 GHz, the simulated NF_{min}, simulated *NF*, and measured *NF*, are 2.84 dB, 2.85

dB, and 2.9 dB, respectively. Figure 75 shows a comparison of the measured *NF* results based on the bias conditions in Table 11. When the SiGe LNA is biased in the WS mode, there is a minor degradation in the noise performance. At 10 GHz in the WS mode, the noise figures at 0.5 mW and 1 mW, are 3.1 dB and 3.2 dB, respectively.

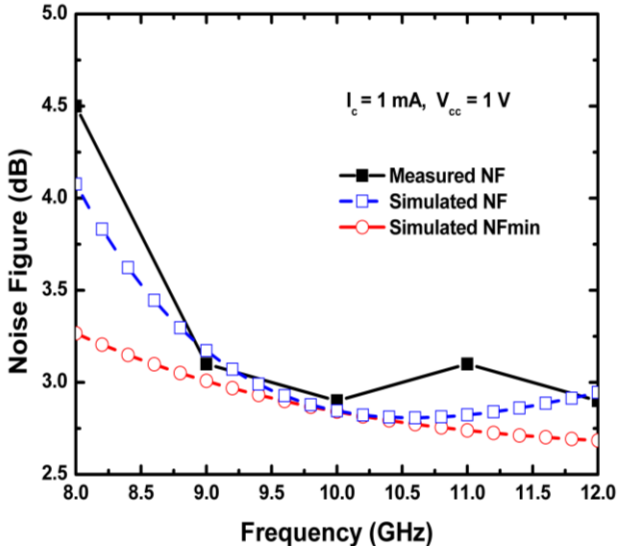


Figure 74: Simulated and measured *NF* results of the SiGe LNA biasing at 1 mW in FA mode.

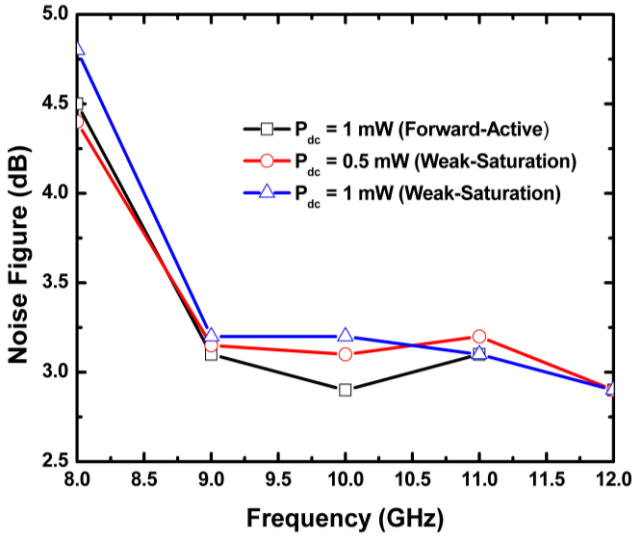


Figure 75: Measured *NF* results of the SiGe LNA at different bias conditions.

6.3.5 Linearity Measurement

A two-tone, input third-order interception point (IIP_3) measurement was performed on the SiGe LNA using the Agilent E4446A Spectrum Analyzer. Two tones with the same amplitude were applied to the LNA at the frequencies 10 GHz and 10.008 GHz. Figure 76 shows the measured IIP_3 results of the LNA at different bias conditions. It is shown that in the FA mode, the IIP_3 of the LNA improves with the increasing I_c from -8.0 to -0.2 dBm. On the other hand, when the LNA is biased in the WS mode, the IIP_3 degrades with the increasing I_c from -6.0 to -9.0 dBm.

Figure 77 shows the measured input P_{1dB} of the SiGe LNA at 10 GHz. Both FA and WS operations show improvements in the P_{1dB} with increasing I_c. The P_{1dB} for the SiGe LNA is ranged from -24.3 to -21.8 dBm for the FA mode, and from -23.8 to -22.8 dBm for the WS mode. Given the same P_{dc} of 1 mW, the WS mode gives a better P_{1dB} performance, as shown in Figure 77.

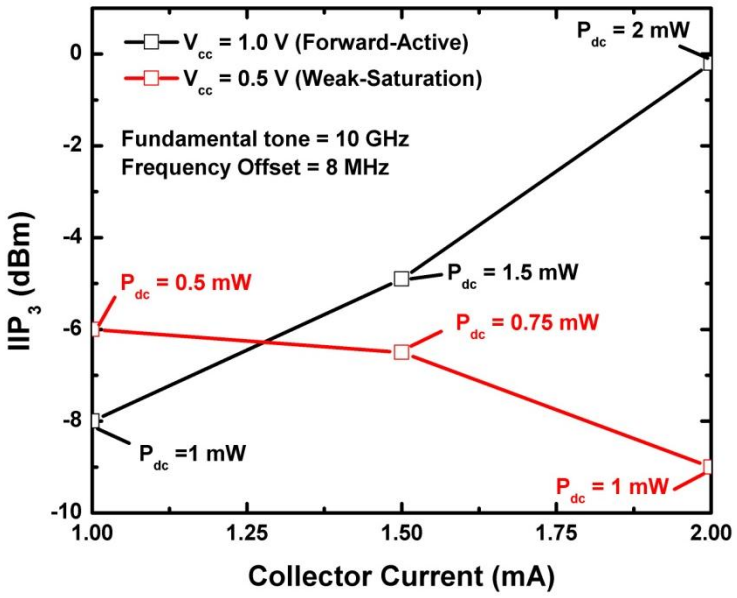


Figure 76: Measured IIP_3 results of the SiGe LNA at different bias conditions.

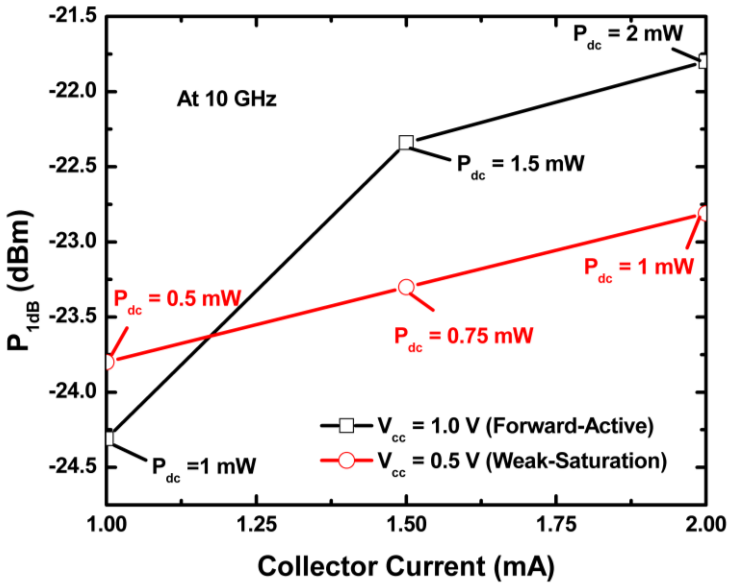


Figure 77: Measured input P_{1dB} results of the SiGe LNA at different bias conditions

6.3.6 Stability

Stability is one of the most important requirements in amplifier design. An LNA that uses a common-emitter configuration has a finite isolation between its input and output, which can potentially lead to stability issues. The stability factor (K) and stability measure (B) are given as

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|}, \tag{69}$$

and

$$B = 1 + |S_{11}|^2 - |S_{22}|^2 - |S_{11}S_{22} - S_{12}S_{21}|^2, \tag{70}$$

where $K > 1$ and $B > 0$ in order for the LNA to be unconditionally stable [66]. Adding a small resistance at the collector of the SiGe HBT helps to improve the LNA stability. Figure 78 shows the simulated plots of the S_{21}, IIP_3, B, and K as R_c varies for the FA SiGe LNA at 10 GHz with I_c = 1 mA and V_{cc} = 1 V. Decreasing the R_c increases the K, but at the same time, it degrades the gain and the IIP_3 of the LNA.

For the SiGe LNA, the R_c was selected to be 250 Ω. As shown in Figure 78, when R_c = 250 Ω, the simulated S_{21}, IIP_3, *B*, and *K*, are about 10.5 dB, -7.4 dBm, 1.1, and 1.4 at 10 GHz, respectively. Figure 79 shows the calculated *K* and *B* through (69) and (70), based on the measured S-parameters as shown in Figure 73. *K* is greater than one and *B* is greater than zero for all the bias conditions across the X-band.

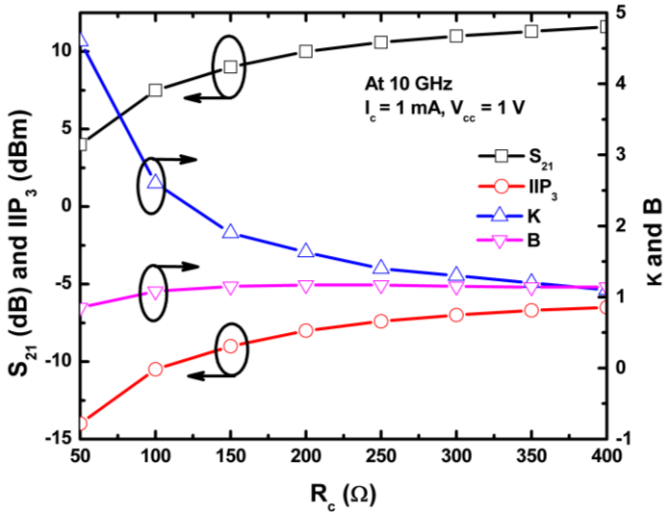


Figure 78: Simulated S_{21}, IIP_3, *B*, and *K* of the SiGe LNA biasing at 1 mW in FA mode.

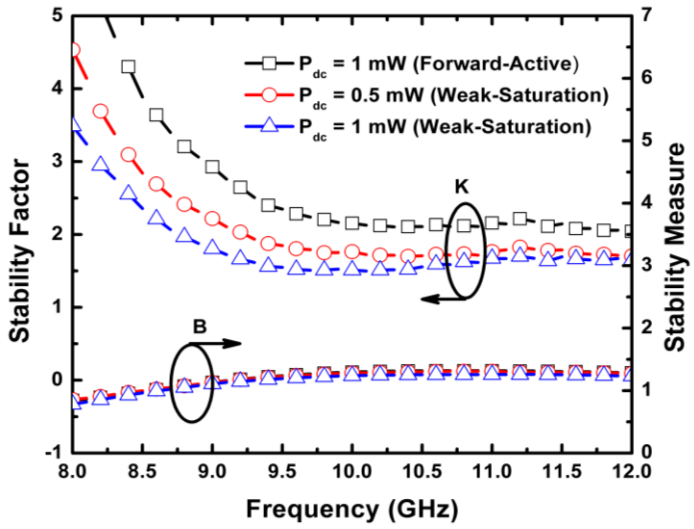


Figure 79: Calculated *K* and *B* of the SiGe LNA for different bias conditions.

6.4 Benchmarking

Table 13 shows a comparison between different X-band LNAs and the present work. Three different FOMs, *FOM1*, *FOM2*, and *FOM3*, are used to benchmark the X-band LNAs listed in Table 13. A higher FOM number represents better LNA performance. The FOMs are expressed as follows:

$$FOM1 = \frac{S_{21}(dB)}{P_{dc}(mW)}, \tag{71}$$

$$FOM2 = \frac{S_{21}(mag)}{[F-1].P_{dc}(mW)}, \tag{72}$$

and

$$FOM3 = 10\log_{10}\left(100.\frac{S_{21}(dB)}{[F-1].P_{dc}(mW)}.\frac{IIP_3(mW)}{P_{dc}(mW)}\right). \tag{73}$$

According to [69], *FOM1* measures the amount of S_{21} in dB achieved per 1 mW of P_{dc}, and *FOM2* normalizes the S_{21} in absolute with respect to the F and P_{dc}. Lastly, *FOM3* compares the overall performance of the LNAs, which includes the gain, F, IIP_3, and P_{dc} [84]-[85]. The SiGe LNA presented in this work exhibits the highest *FOM1*, *FOM2*, and *FOM3*, when it is biased in WS mode at 0.5 mW. Even though the proposed LNA uses a lower peak f_T HBT in the design, it is still able to deliver very good gain at low P_{dc}. Figure 80 compares the performance of the LNAs using FOM3 against P_{dc}.

Table 13: Comparison with other SiGe low-noise amplifiers.

Reference	Frequency (GHz)	P_{dc} (mW)	Vcc (V)	Gain (dB)	NF (dB)	IIP_3 (dBm)	Size (mm^2)	Technology	*FOM1* (dB/mW)	*FOM2* (mW^{-1})	*FOM3*
This work[+]	**10**	**0.5**	**0.5**	**8.5**	**3.1**	**-6.1**	**0.56**	**150 GHz SiGe HBT**	**17.04**	**5.12**	**29.05**
This work[+]	**10**	**1**	**0.5**	**11.0**	**3.2**	**-9.0**	**0.56**	**150 GHz SiGe HBT**	**11.00**	**3.26**	**21.04**
This work[++]	**10**	**1**	**1**	**9.0**	**2.9**	**-7.86**	**0.56**	**150 GHz SiGe HBT**	**9.05**	**2.98**	**21.93**
This work[++]	**10**	**2**	**1**	**11.5**	**3.2**	**-0.4**	**0.56**	**150 GHz SiGe HBT**	**5.75**	**1.73**	**23.81**
[67]	9.5	2.5	2.5	11	2.78	-9.1	0.51	180 GHz SiGe HBT	4.40	1.58	13.83
[68]	10	15	2.5	19.5	1.36	0.8	0.53	200 GHz SiGe HBT	1.30	1.71	14.52
[69]	10	2	1.5	10	1.98	0	0.43	200 GHz SiGe HBT	5.00	2.74	26.36
[77]	9	2.4	1	16.7	3.5	-6	0.75	200 GHz SiGe HBT	6.96	2.30	17.69
[86]	9.6	18	1.8	18	4	-11.3	1.44	180 nm SiGe BiCMOS	1.00	0.29	-5.65
[87]	10	13.7	1.8	10	4.8	-6	0.8	180 nm CMOS	0.73	0.11	-1.79
[88]	10	1.8	1.2	14	3.5	-18	0.74	200 GHz SiGe HBT	7.78	2.25	7.43

[+] Weak-saturation mode
[++] Forward-Active mode

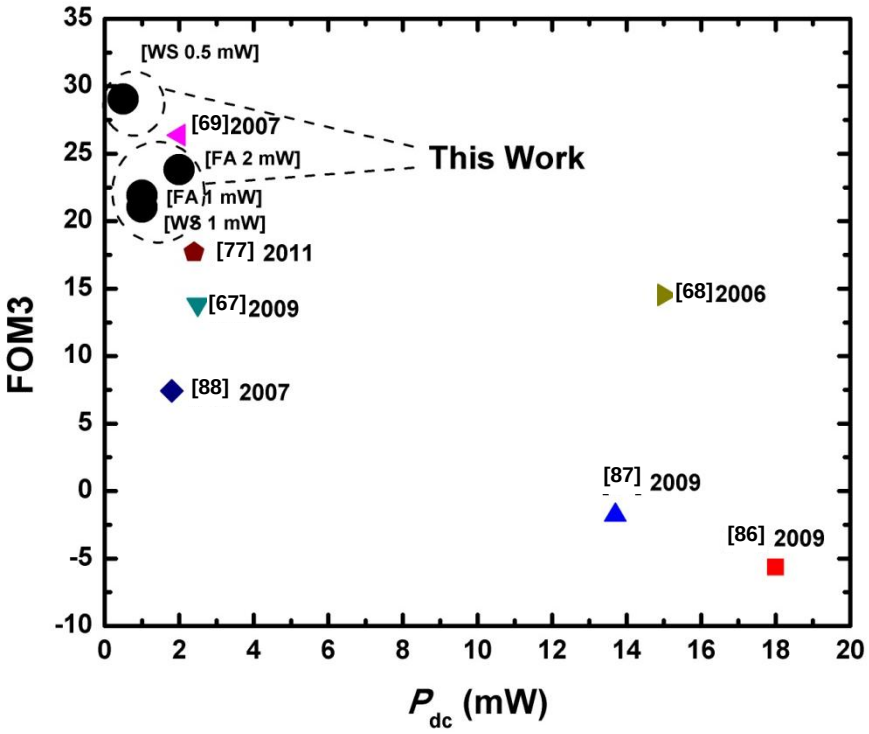


Figure 80: Performance comparison graphs using *FOM3* against P_{dc}.

6.5 Summary

This dissertation has presented a low-power and low-voltage X-band SiGe LNA. The SiGe LNA was implemented using a 200 nm, 150 GHz peak f_T SiGe HBT BiCMOS process technology. For the first time, a direct comparison of RF performance was made between the forward-active (FA) and weak-saturation (WS) modes. Measurement shows that by driving the SiGe LNA in the WS region, the *dc* power consumption of the LNA improves without major degradation to the gain and noise performance. Given the same power consumption of 1 mW, the WS mode has a higher gain and a higher P_{1dB} than the FA mode. When the SiGe LNA is biased in WS mode at 0.5 mW and V_{cc} = 0.5 V, the SiGe LNA has a gain of 8.5 dB at 10 GHz, and a peak gain of 9.7 dB at 8.7 GHz, making this the highest gain per *dc* power consumption X-band SiGe LNA reported to date. The proposed low-power SiGe LNA achieves excellent FOMs when compared to other X-band LNAs, and represents a state-of-the-art solution for the next generation of wireless communication systems.

CHAPTER VII

X-BAND TO KA-BAND SPDT SWITCH USING 200 NM SIGE HBTS

7.1 Introduction

RF switches are key elements for any transceiver system. It is important that the switch has a low insertion loss and provides high isolation between the transmitter and receiver in order to minimize potential interference. However, it is often difficult to implement broadband transceivers because of the bandwidth limitation of requisite RF switches. RF microelectromechanical system (MEMS) technology has been used to design broadband switches with very low insertion loss [89], but their applications are limited because they require a very high actuation voltage and have not yet been integrated on a commercial circuit platform. A broadband CMOS switch up to 50 GHz has been reported in [90]. However, the switch design uses a traveling-wave concept which usually requires large die area. PIN diode based broadband switches [91] implemented in SiGe technology have shown excellent RF performance from 1 to 20 GHz, but these diode-based switches consume a large amount of power (>20 mW), which is undesirable for wireless applications.

In this dissertation, the design of a broadband SPDT switch using a 200 nm, 150 GHz peak f_T SiGe HBT BiCMOS process technology (Jazz SBC-18) is presented. The proposed SiGe SPDT switch uses diode-connected SiGe HBTs that have very broadband characteristics. The design utilizes a series-shunt configuration, which further improves the isolation. Between 8 and 40 GHz, this SiGe SPDT switch has an insertion loss of less than 4.3 dB and an isolation of more than 20.3 dB, and consumes only 5.6 mW of power. To the best of the author's knowledge, the proposed SiGe SPDT switch has the broadest operating bandwidth of any SiGe SPDT switch that has been reported to date.

7.2 SPDT Switch Design

Figure 81 shows the schematic of a single diode test structure. The test structure consists of two RF chokes for *dc* biasing, and two *dc* blocks at the input and output. The diode is formed by shorting the base and collector terminals of a SiGe HBT. The impedance of a diode-connected HBT is given by

$$Z_D = \frac{1}{j\omega(C_\pi + C_s) + \frac{\beta + 1}{r_\pi}}, \tag{74}$$

where C_π, C_s, β, and r_π, represent the base-emitter capacitance, collect-substrate capacitance, forward current gain, and base-emitter resistance, respectively [92].

For this SPDT design, the emitter stripe width of the diode-connected SiGe HBT is 0.2 μm. By increasing the emitter length, the r_π of the HBT decreases [20] and hence Z_D also decreases. Therefore, a large emitter length is preferred for switch design to create a low-impedance SiGe HBT. Figure 82 shows the simulated S_{21} and S_{11} results of the single diode test structure with different emitter lengths. The diode is forward-biased by supplying a *dc* voltage of 0.9 V at V_{in}. As expected, the SiGe HBT with the longest emitter length (10.16 μm) shows the lowest insertion loss and best impedance match.

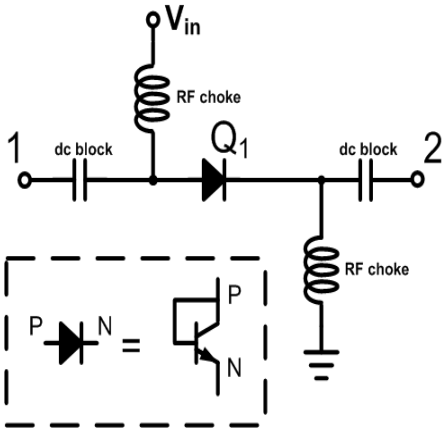


Figure 81: Schematic of a single diode test structure.

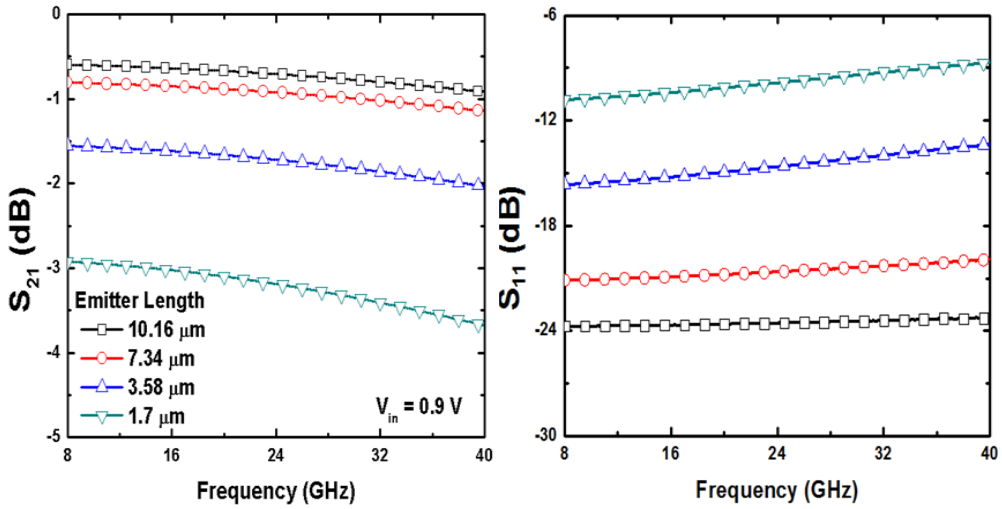


Figure 82: Simulated S_{21} (left) and S_{11} (right) for different emitter lengths.

After the emitter length of the diode is selected, the V_{in} in Figure 81 can be swept to determine the optimum control voltage for biasing the diode. This diode shows the least insertion loss when V_{in} is set at 0.95 V, as shown in Figure 83.

Figure 84 shows the schematic of a single-pole single-throw (SPST) switch configuration. The SPST switch consists of series and shunt elements. The SiGe HBT in the shunt element has the same device size as in the series element. To turn on the RF path between port 1 and 2, input A has to be set to 0.95 V and input B to 0 V. To turn off the RF path, the input voltages are interchanged. Figure 85 shows a comparison of the insertion loss and isolation between the series (without the shunt element) and series-shunt configurations (with the shunt element).

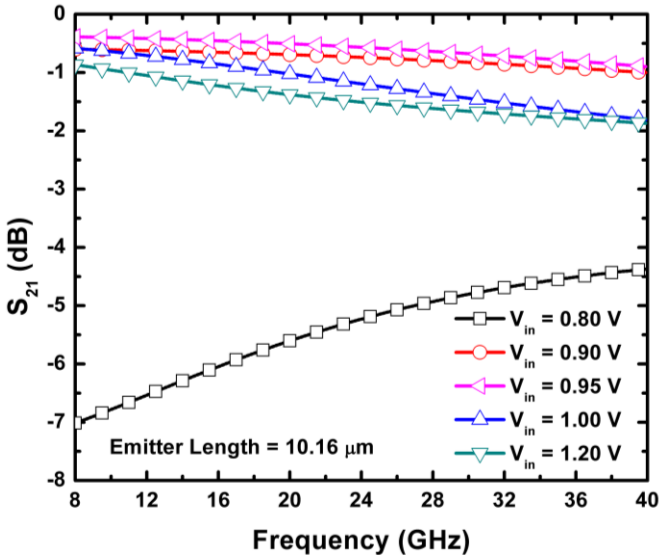


Figure 83: Simulated S_{21} for different values of V_{in}.

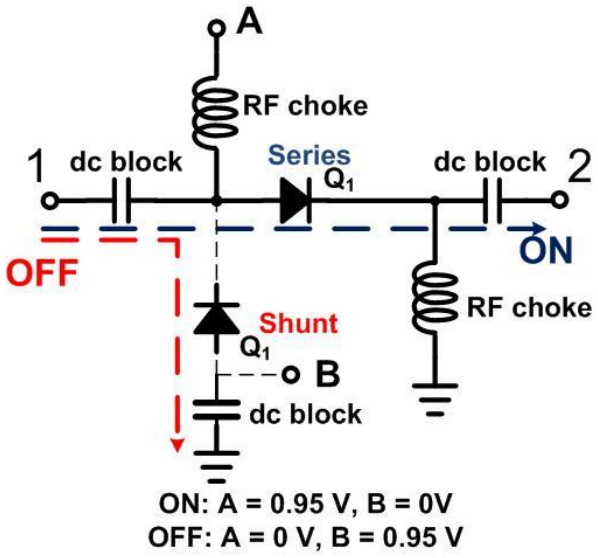


Figure 84: Schematic of a SPST switch.

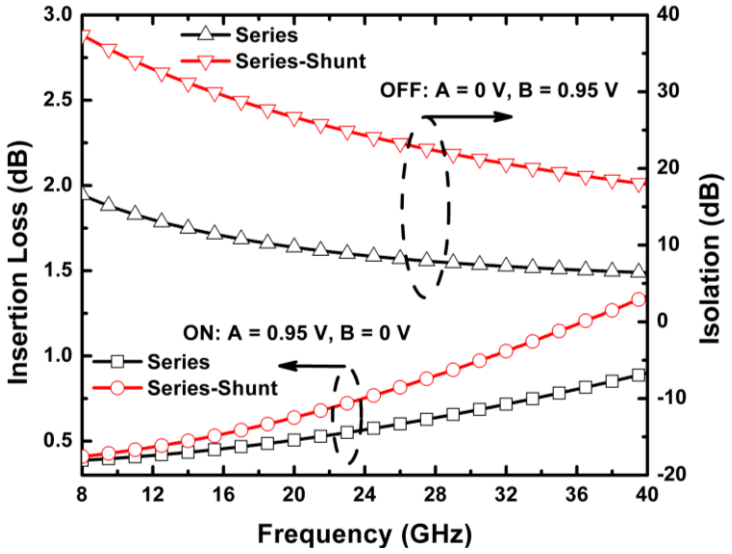


Figure 85: Simulated insertion loss and isolation of the SPST switch, series and series-shunt configurations.

Between 8 and 40 GHz, when the SPST switch is "on", the series configuration has an insertion loss of about 0.38 to 0.9 dB. The insertion loss is about 0.41 to 1.35 dB for the series-shunt configuration. When the SPST switch is "off", the worst-case isolation occurs at 40 GHz. At 40 GHz, the series and series-shunt configurations have isolation of 6.4 dB and 17.9 dB, respectively. Therefore, implementing a series-shunt configuration in the switch design helps to improve the isolation by more than 11.5 dB, with minimal degradation (< 0.45 dB) of the insertion loss.

Figure 86 shows the schematic of the proposed SiGe SPDT switch. When the diode is forward-biased, it draws *dc* current from the voltage source, and thus consumes power. To minimize this power drain, limiting resistors (R_1) are added to the SPDT switch. Figure 87 shows the simulated S_{21} and the power consumption of the SPDT switch with different values of R_1. By increasing the resistance of R_1, the amount of *dc* power consumed by the SPDT switch reduces, but the insertion loss degrades, presenting a tradeoff.

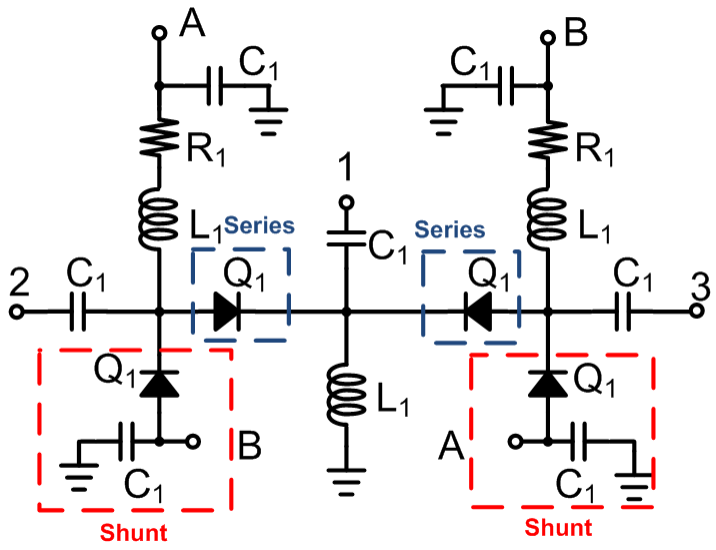


Figure 86: Schematic of the SPDT switch.

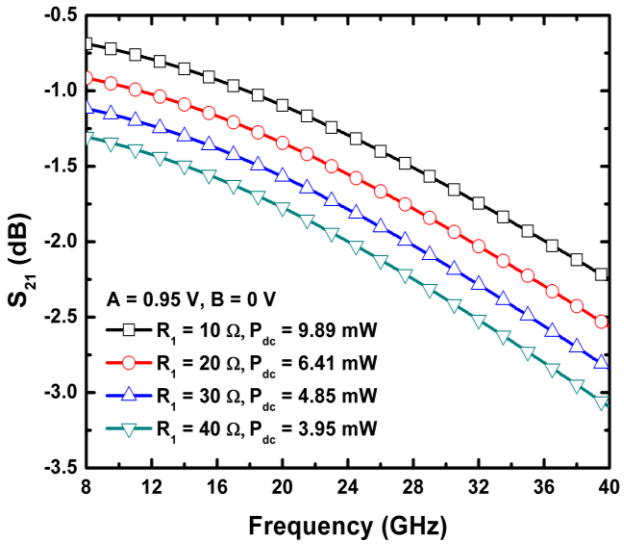


Figure 87: Simulations of S_{21} and *dc* power consumption for different values of R_1.

For the SPDT switch, R_1 was selected to be 12 Ω. Between 8 and 40 GHz, the simulated S_{21} of the SPDT switch is about -0.73 to -2.31 dB, with 8.88 mW consumed. The value of the capacitance C_1 in Figure 86 is 1 pF. The value of inductance L_1 was selected to match the SPDT switch to a 50 Ω impedance. Figure 88 shows the simulated

S_{11} for different values of L_1. Ideally, the valley of the S_{11} should be near the center frequency at 24 GHz to ensure a broad impedance match between 8 and 40 GHz. Using the simulation results in Figure 88, L_1 was selected to be 1.2 nH.

7.3 Measurement

Figure 89 shows the photomicrograph of the fabricated SPDT switch, which has a dimension of 1.38 x 0.99 mm^2 (0.48 x 0.41 mm^2 not including the pads). The actual power consumption measured for the SPDT switch was 5.6 mW, because of additional parasitic resistances introduced by the layout. A post-extraction simulation was performed and the *dc* power consumed by the SPDT switch was simulated to be 5.9 mW, in good agreement with the data.

The S-parameter measurements were performed with an Agilent E8363B VNA from 8 to 40 GHz using ground-signal-ground (GSG) co-planar microwave probes of 150 μm wide pitch. The VNA was calibrated using a four-port short-open-load-thru (SOLT) standard. Figure 90 shows the measured and post-extraction simulated S-parameter results for the SiGe SPDT switch. Table 14 shows the measured insertion loss and isolation of the SPDT switch from 8 to 40 GHz. The measured S_{11} is less than -9.6 dB and the measured S_{22} is less than -9 dB. The measured isolation between Port 2 and Port 3 is more than 22 dB from 8 to 40 GHz (not shown).

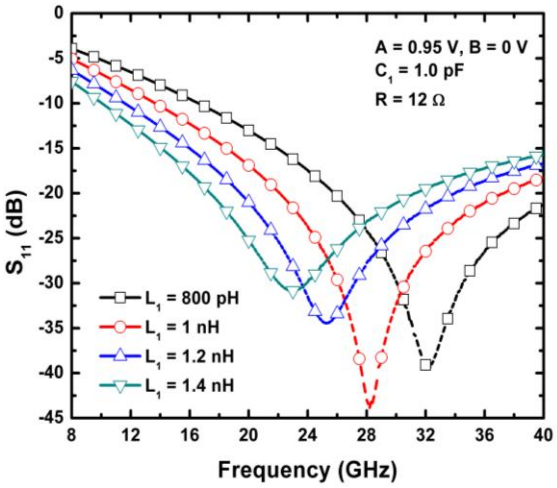


Figure 88: Simulations of S_{11} for different values of L_1.

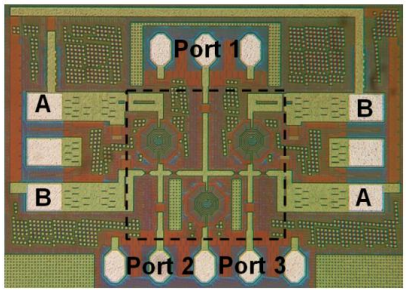


Figure 89: Photomicrograph of the SPDT switch, with the switch core highlighted in the middle.

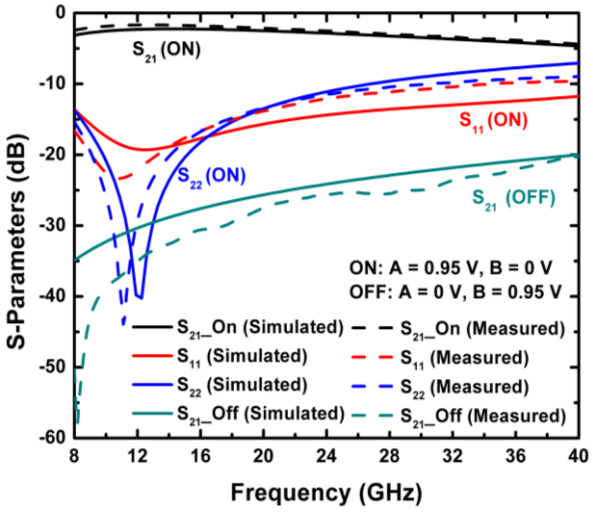


Figure 90: Simulated and measured S-parameter results for the SiGe SPDT switch.

The two-tone, IIP_3 and the input-referred P_{1dB} of the SPDT switch were measured using an Agilent E4446A Spectrum Analyzer. With a two-tone spacing ΔF of 8 MHz, the extrapolated IIP_3 points are 21 dBm and 19 dBm, at fundamental frequencies of 10 GHz and 20 GHz, respectively. Figure 91 shows the measured IIP_3 results. The measured P_{1dB} is about 11.06 dBm and 9.72 dBm, at 10 GHz and 20 GHz, respectively (not shown).

A comparison of the present work with other broadband SPDT switches is summarized in Table 15. This comparison demonstrates the potential of designing a low insertion loss and high isolation SPDT switches over an extremely wide range of frequencies using diode-connected SiGe HBTs in a series-shunt configuration.

Table 14: Measured insertion loss and isolation.

Frequency (GHz)	I.L (dB)	ISO (dB)
8 to 12 (X-band)	2.4 to 1.6	58 to 35
12 to 18 (Ku-band)	1.6 to 1.9	35 to 29.5
18 to 26 (K-band)	1.9 to 2.7	29.5 to 25.3
26 to 40 (Ka-band)	2.7 to 4.3	25.3 to 20.3

I.L – Insertion Loss, ISO – Isolation

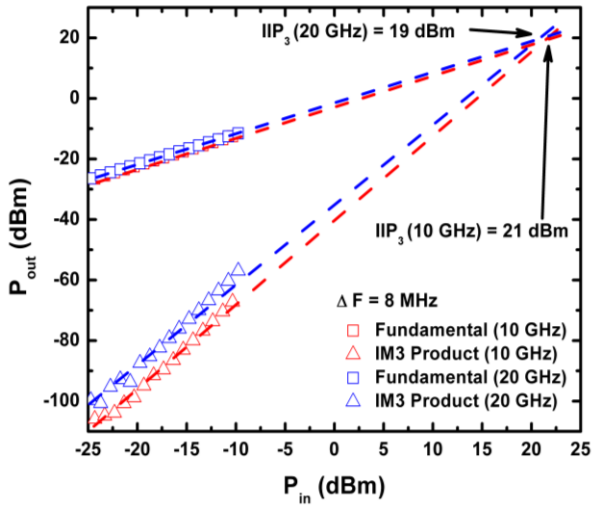


Figure 91: Measured IIP_3 results for the SiGe SPDT switch at 10 GHz and 20 GHz.

Table 15: Performance comparison between other broadband SPDT switches.

Reference	Frequency (GHz)	I.L (dB)	ISO (dB)	R.L (dB)	P_{1dB} (dBm)	IIP_3 (dBm)	Size (mm^2)	Control Voltage (V)	Technology
This work	**8 to 40**	**1.6 to 4.3**	**20.3 to 58**	**> 9**	**10**	**20**	**0.20 / 1.4$^+$**	**0.95**	**200 nm SiGe HBT**
[93]	8 to 20	1.4 to 2.0	> 15	> 15	12.5	22.5	0.29	1.2	130 nm SiGe BiCMOS
[94]	10 to 18	< 1.9	> 22	> 13	21	> 30	0.005	NR	180 nm SiGe BiCMOS
[95]	15 to 50	< 3.1	> 40	> 8	NR	NR	3$^+$	1.5	100 nm GaAs pHEMT
[96]	2 to 18	< 4	> 15	NR	34.4	NR	9.92$^+$	10	GaN HEMT
[97]	0 to 20	0.5 to 2.5	25 to 60	> 9	> 19.8	> 31.5	0.06	1.8 / 3.6	180 nm CMOS

+ With Pads; NR – Not Reported; R.L – Return Loss

7.4 Summary

This dissertation has presented a broadband X-band to Ka-band SPDT SiGe switch. The SPDT switch was implemented using 200 nm, 150 GHz peak f_T SiGe HBT BiCMOS process technology. This work has demonstrated the feasibility of using the diode-connected SiGe HBTs in a series-shunt configuration to improve the switch bandwidth and achieve high isolation. Between 8 and 40 GHz, the SPDT switch has an insertion loss of less than 4.3 dB, an isolation of more than 20.3 dB, and a return loss of more than 9 dB, while consuming a *dc* power of only 5.6 mW. In addition, this SPDT switch has a 3 dB bandwidth of more than 32 GHz, making this the broadest bandwidth of any SiGe SPDT switch currently reported.

CHAPTER VIII

PACKAGING EFFECTS OF MULTIPLE X-BAND SIGE LNAS EMBEDDED IN AN ORGANIC LCP SUBSTRATE

8.1 Introduction

For high-frequency integrated circuits, the selection of packaging is critical, because the package interconnects can directly influence the overall system performance. It is extremely important to minimize any parasitic associated with the package interconnects, so that the circuit can perform as intended. In addition, the package interconnect should be well-modeled, so that the circuits can be optimized, integrated, and evaluated, to enhance the system performance.

As shown in Figure 92a, the wirebond interconnect [98] is convenient to implement, but as frequency increases, the bond wire tends to introduce more loss and impedance mismatch to circuits, limiting their high-frequency applications. LCP organic substrate has been widely used as a packaging material for many RF and microwave applications, because of its high-performance electrical and mechanical properties [54,99,100]. X-band SiGe LNAs have been successfully embedded inside multi-layer LCP substrates [101], as shown in Figure 92b. In this case, the LCP is laminated over the SiGe LNA and an excimer laser is used to bore holes in the LCP so that the LNA pads are exposed and via interconnects can be formed. This packaging approach has shown excellent RF characteristics, but it is difficult to implement for a multichip module (MCM), because there is a high chance of via-pad misalignment, especially when involving multiple die and via interconnects in a single package. Alternatively, embedded flip-chip shown in Figure 92c, is an attractive packaging alternative for high-frequency applications [102]. Flip-chip technology has excellent electrical properties up to 100 GHz and requires very low assembly costs [103].

Few studies have been performed to evaluate and compare the effects of

embedded flip-chip and wirebond interconnect parasitics on performance of RF circuits, especially at high frequencies. Furthermore, multiple die are seldom used in a single package for comparing the packaging effects, which is critical for most MCM applications. Previously [104], CMOS LNAs were used to compare the flip-chip and wirebond packaging effects on RF performance at 2.4 GHz. However, at this low frequency, packaging effects are not that significant, thus making it difficult to make a strong comparison. In addition, in [105], transmission lines and Schottky diodes were used instead to evaluate the performance of the flip-chip and wirebond interconnects. As the transmission lines and Schottky diodes have very broadband characteristics, any packaging induced degradations (e.g. frequency shift / impedance mismatch) would be difficult to discern. So far, much of the existing interconnect modeling literature focuses on the transition effects and electrical characterization [106,107,108]. The utilization of these models to simulate multiple die integrated into a single package are rarely compared with measured data.

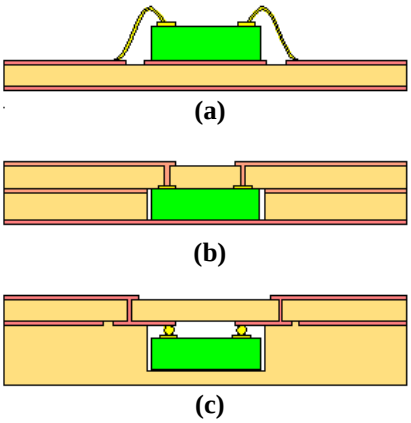


Figure 92: Different types of RF packages: (a) wirebonded package, (b) embedded die package, and (c) embedded flip-chip package.

In the dissertation, for the first time, X-band SiGe LNAs are used to evaluate the effects of different RF packaging approaches on circuit performance. The SiGe LNAs were designed to operate at 9.5 GHz. Any impedance mismatch caused by the package interconnects can be easily shown through S-parameter measurements. In addition, two SiGe LNAs were embedded inside a multilayer LCP substrate and combined together using a novel modified Wilkinson power combiner. This approach was taken to address the potential issues of embedding multiple die together in a single package. Fabricating a standard Wilkinson power combiner on a thin substrate can be challenging as the line width gets narrow. The proposed modified Wilkinson power combiner helps to overcome this concern and ease the fabrication process, making the design more realizable. Finally, this work addresses the issue of interconnect modeling. Using the models in circuit simulations helps to predict circuit performance with greater accuracy and to compensate for parasitic-induced losses accordingly. Simulations are very useful in such situations, where hundreds of package interconnects are involved and EM simulations are impractical or impossible.

8.2 X-Band SiGe LNA

The X-band SiGe LNA was fabricated in a seven-metal-layer, commercial-available, 200 GHz, 130 nm SiGe BiCMOS process technology (IBM 8HP). As shown in Figure 93, the SiGe LNA was designed using a cascode configuration to reduce the Miller effect, increase the reverse isolation, and improve the circuit stability [68]. At 9.5 GHz, the LNA has a measured gain of 20.7 dB, a return loss of more than 20 dB, and a noise figure of less than 2 dB.

Figure 94 shows a photomicrograph of the SiGe die, where the LNA is located in the center, with other test structures around the sides. Including the bondpads, the die size is 4.5 x 3.0 mm^2. For the wirebonded package, the SiGe LNA has to be diced out to a size

of 830 x 700 μm^2 so that the bond wire length can be shortened. On the other hand, for the embedded flip-chip package, dicing is not required. In addition, the SiGe LNA does not have a ground plane underneath its die and there will not be any floating ground issues when using flip-chip bonding.

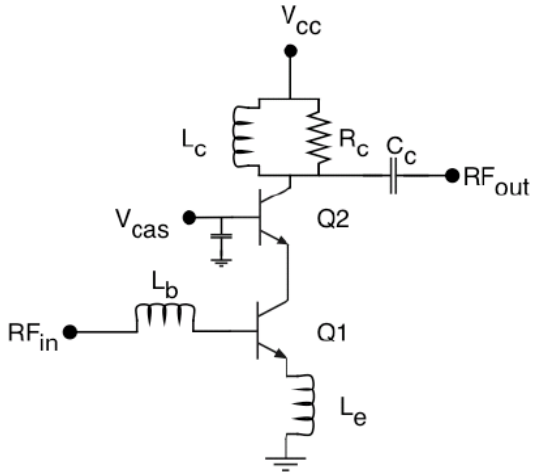


Figure 93: Schematic of the cascode SiGe LNA used in this work.

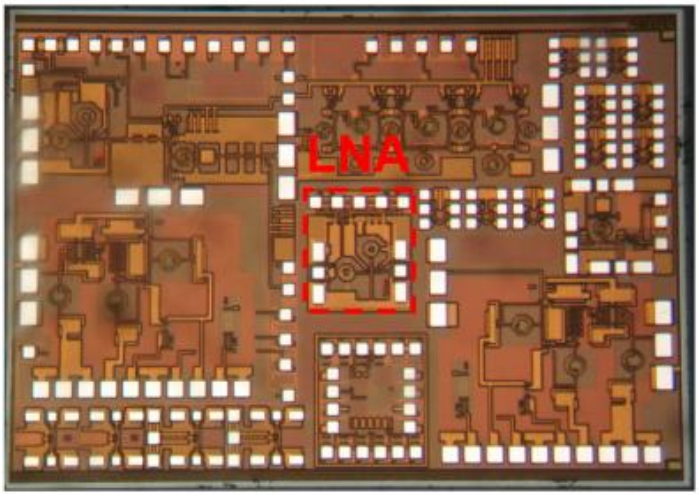


Figure 94: Photomicrograph of SiGe die with the LNA highlighted in the center.

8.3 Interconnect Transitions

The SiGe LNA pads were designed in a ground-signal-ground (GSG) configuration. The signal and ground pads of the SiGe LNA were bonded directly to the LCP CPW line. The parameters of the CPW line are shown in Table 16. The LCP board also has ground vias that connect the top and bottom ground planes. The spacing between each via is less than one-tenth of the wavelength in the dielectric, in order to minimize the potential difference between the ground planes.

For the wirebonded package, SiGe LNAs were epoxy-attached to a copper base on the LCP. The gap between the copper base and the CPW line is about 172 µm. The wire diameter is about 25.4 µm. For each wire, the horizontal distance between the first and second bonds is about 700 µm. With loop height of 127 µm and die thickness of 316 µm, the total length of the wire is estimated to be 960 µm long. The RF signal and ground flow from the LCP CPW line into the SiGe LNA pads through the wirebond interconnects as shown in Figure 95. As the signal wire is between the two ground wires, the electromagnetic field is partially confined, which helps to minimize potential crosstalk.

Table 16: LCP CPW parameters.

Parameter	Value
Type	Conductor-backed CPW
Dielectric constant, ε_r	2.95
Dissipation factor (Tan δ)	0.0025
Substrate thickness (mil)	2
Conductor thickness (µm)	9
CPW line width (µm)	109
CPW signal-ground gap (µm)	50
Characteristic impedance, Z_o (Ω)	50

For the embedded flip-chip package, the LCP substrate has CPW lines fabricated on the top and bottom layers. The CPW lines are connected through a 120 µm diameter via [109]. Gold (Au) bumps are added to the SiGe LNA pads using a thermosonic attachment process [110]. By using combination of heat, pressure and ultrasonic energy, the Au bumps are attached firmly to the pads. Each Au bump is about 35 µm in height and 55 µm in diameter. The SiGe LNA dies are then flipped onto the bottom CPW line. The RF signal and ground flow from the top CPW line to the bottom CPW line through the vias as shown in Figure 96. The RF signal and ground are then flowed into the SiGe LNA pads through the Au bumps.

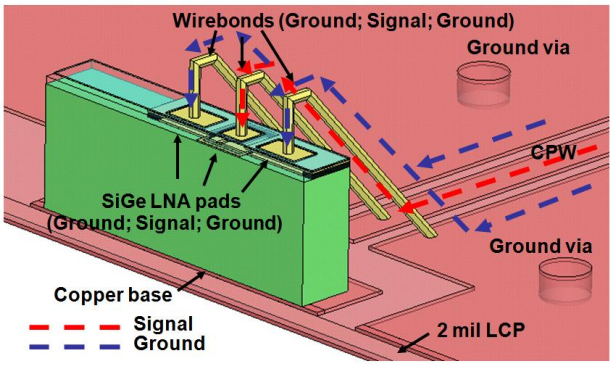


Figure 95: Signal-flow between the CPW and the SiGe LNA through the wirebond interconnect.

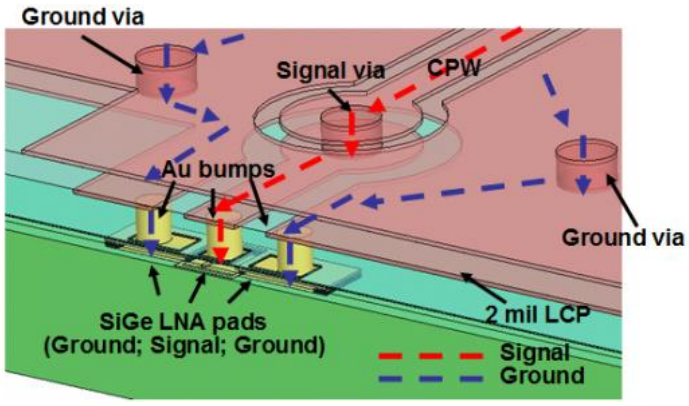


Figure 96: Signal-flow between the CPW and the SiGe LNA through the flip-chip interconnect.

Au bumps on the LNA pads have to be properly placed, so that pads and the CPW lines can properly align. The SiGe LNA has a wider ground pads than the signal pads. The Au bumps on the ground pads are placed apart from signal pads, as shown in Figure 97, to avoid shorting of signal during the bonding process. Figure 98 shows the photomicrograph of the Au bumps on a SiGe die with the LNA in the center. Figure 99 shows the general process flow for assembling the embedded flip-chip package. The flip-chip SiGe LNA is completely embedded inside the LCP by laminating a multilayer LCP lid that has a machined cavity to fit in the entire die. The fabrication techniques and further details are discussed in [102].

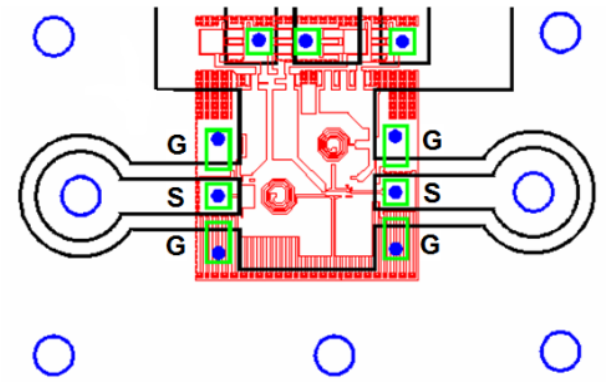
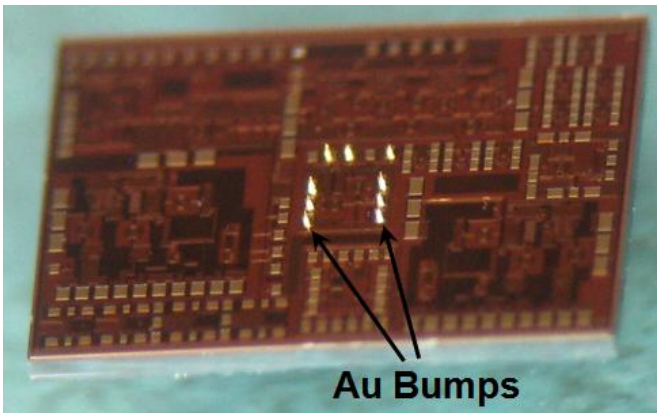
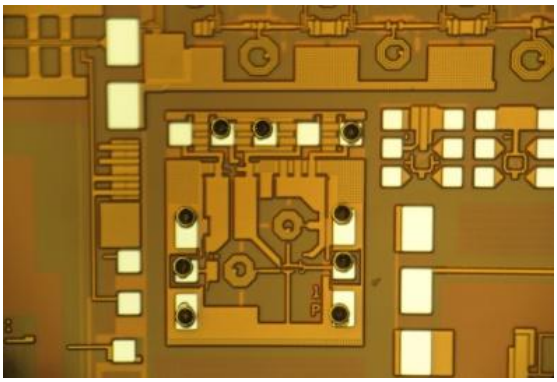


Figure 97: Placement of the Au bumps on the SiGe LNA pads. The red lines represent the SiGe LNA, the green lines represent the pads, the black lines represent the LCP CPW lines, the blue circles represent the LCP vias, and the blue dots represent the Au bumps.



(a)



(b)

Figure 98: Photomicrograph of Au Bumps on the SiGe die: (a) angled view and (b) top-down view of the bump bonded SiGe LNA.

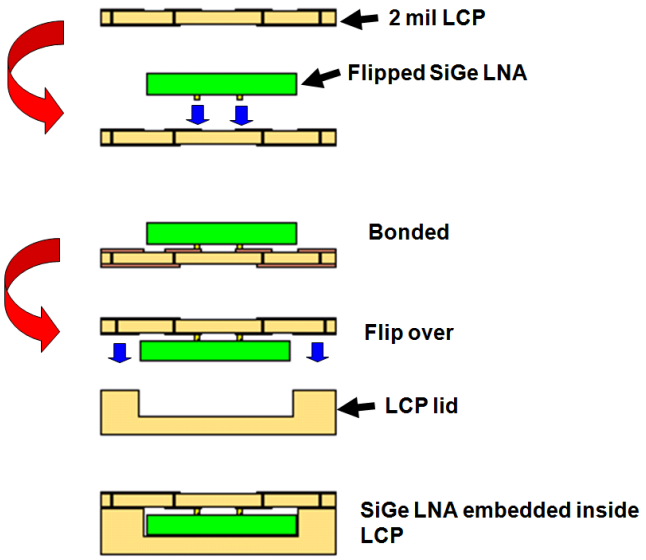


Figure 99: Assembling the embedded flip-chip package.

8.4 Single SiGe LNA

S-parameter measurements were performed using an Agilent E8363B VNA with on-wafer GSG probes (GGB Model 40A), from 8 to 20 GHz. The calibration was done with probe-level SOLT standard on GGB industries CS-5 calibration substrate. Figures 100 and 101 show the LCP packages used for a single X-band LNA, the wirebonded and the embedded flip-chip (without the lid), respectively. The S-parameter measurements were performed on the top side of the LCP with the RF probe tips making contact near the end of each CPW line.

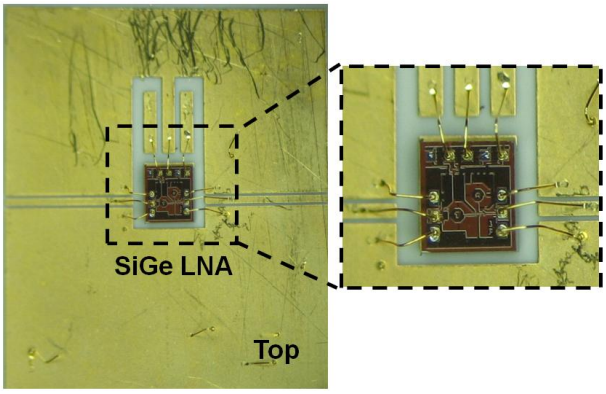


Figure 100: Wirebonded package for a single SiGe LNA.

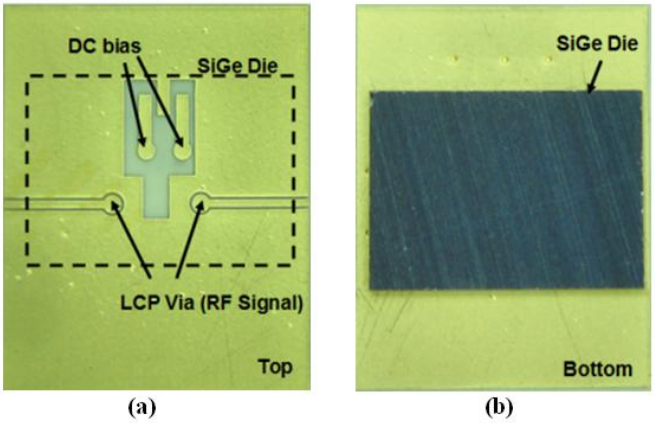


Figure 101: Embedded flip-chip package for a single SiGe LNA: (a) top view and (b) bottom view (without the LCP lid).

Figure 102 shows the measured S-parameters of a single X-band SiGe LNA in wirebonded and embedded flip-chip packages. The wirebonded package induces an additional insertion loss of 2.2 dB, while the embedded flip-chip package induces about 0.4 dB. The valleys of S_{11} and S_{22} for the wirebonded package have shifted down in frequency. On the other hand, there is no major frequency shift in the embedded flip-chip package. In addition, the input return loss for the embedded flip-chip package degrades slightly by 5 dB, but it is still able to maintain a good impedance match with S_{11} less than -15 dB at 9.5 GHz. As shown in Figure 102, the embedded flip-chip package has a better match and its performance is more predictable than the wirebonded package. From 8 to 16 GHz, the degradation in the embedded flip-chip package is less than 1 dB.

Clearly, the embedded flip-chip package proves to be a better candidate than the wirebonded package for X-band applications, since the packaging effects due to the embedded flip-chip package are almost negligible.

8.5 Two SiGe LNAs

8.5.1 Phased-Array Receiver Front-Ends

A phased-array receiver generally consists of multiple LNAs and phase shifters, where the signal phase of each antenna element can be varied independently to steer the antenna beam in a desired direction [111]. As shown in Figure 103, the LNAs and phase shifters are usually designed on-chip, while the antennas and the Wilkinson power combiners are typically designed off-chip. The interconnects between on-chip and off-chip elements are usually achieved using wirebonds [111].

This section focuses on package interconnects for multiple on-chip elements in a system. The test structures shown in Figure 104 are used to compare the wirebond and embedded flip-chip packages, where two SiGe LNAs are combined through a Wilkinson

power combiner, similar to a two-element phased-array receiver without the antennas and phase shifters

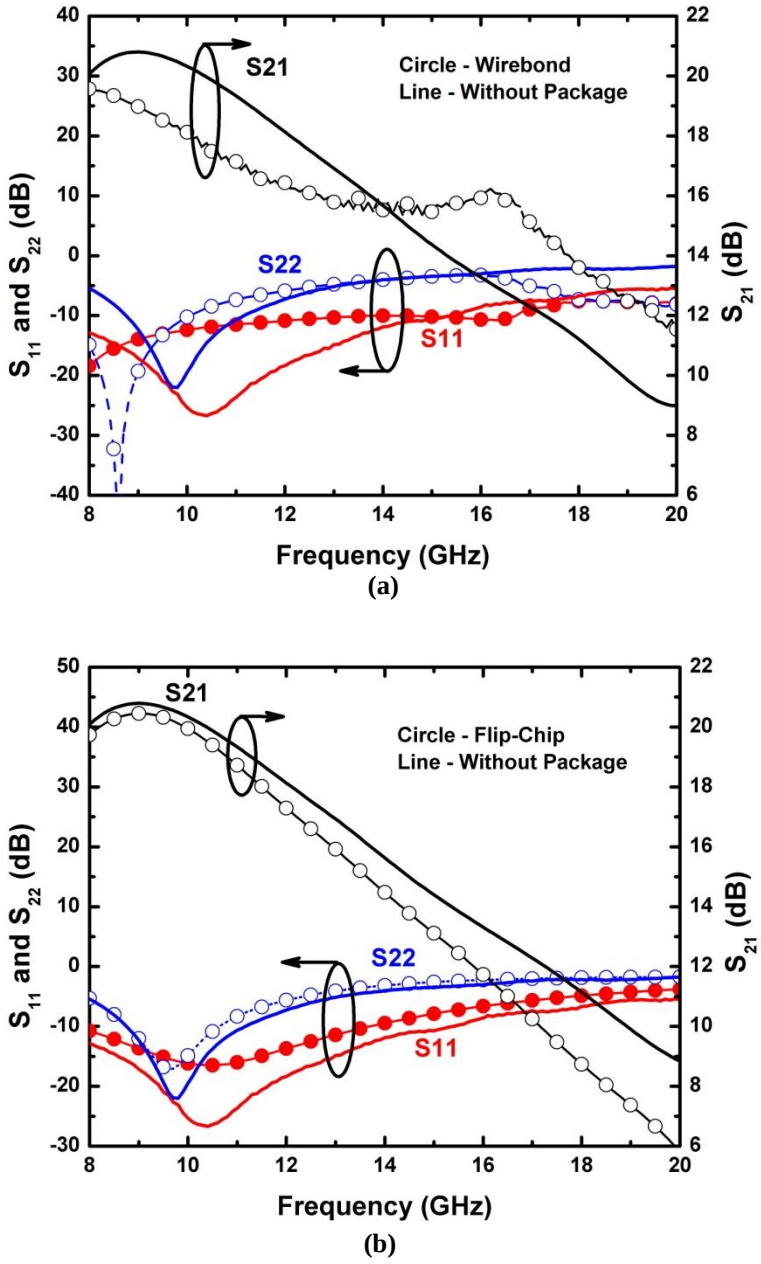


Figure 102: Measured S-parameter results of the single SiGe LNA packages: (a) magnitude of the wirebonded package in dB and (b) magnitude of the embedded flip-chip package in dB.

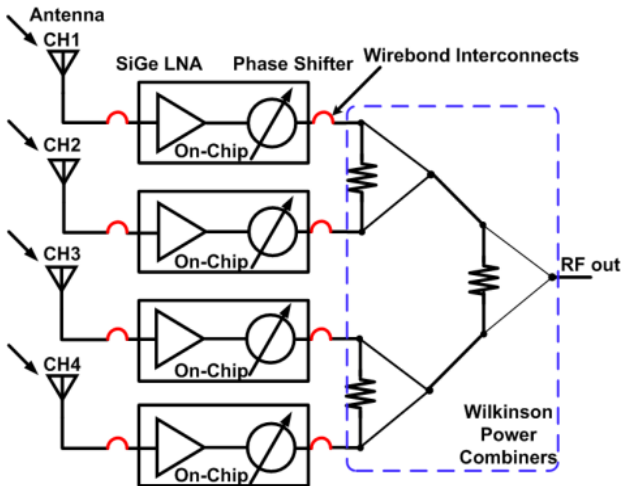


Figure 103: Phased-array receiver front-ends.

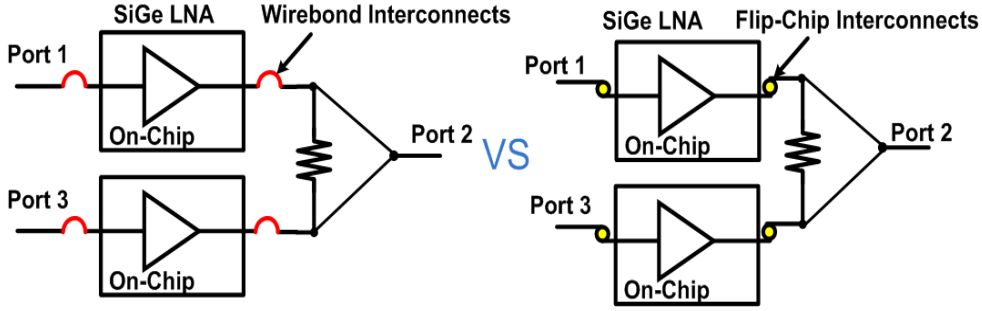


Figure 104: Block diagram of packaging comparison structures for two SiGe LNAs combining through a Wilkinson power combiner.

8.5.2 Novel Modified Wilkinson Power Combiner

Two SiGe LNAs are combined through a novel modified Wilkinson power combiner as shown in Figure 105. Table 17 shows the parameters of the Wilkinson power combiner. The 70.7 Ω transmission line width is 64 µm wide, which is very narrow and thus difficult to fabricate. Hence, the 70.7 Ω transmission lines in the modified Wilkinson power combiner were replaced by wider 50 Ω transmission lines (122 µm). In addition, the combining arm of the modified Wilkinson power combiner consists of a 35.4 Ω quarter-wave transformer (207 µm wide), so that all the three ports are matched to 50 Ω.

This technique helps to ease the fabrication, making the design inherently more manufacturable.

The modified Wilkinson power combiner was analyzed using the even-odd mode analysis [112]. Figure 106 shows the even-mode and odd-mode excitation for the modified power combiner with all impedances normalized to 50 Ω. For the even-mode excitation, it is assumed that

$$V_{port1} = V_{port3} = 2V_o, \tag{75}$$

while for the odd-mode excitation,

$$V_{port1} = -V_{port3} = 2V_o. \tag{76}$$

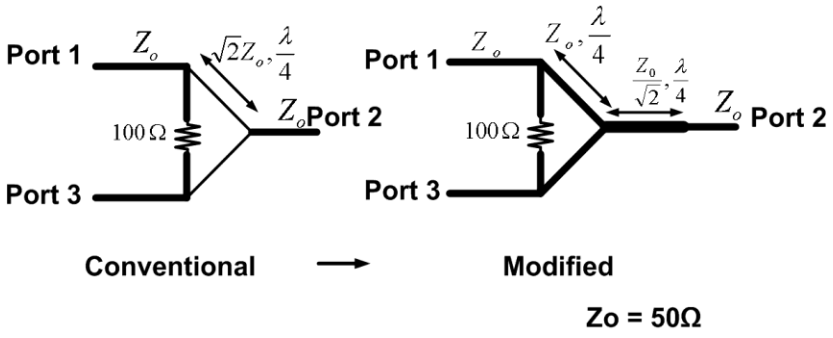


Figure 105: Transition from conventional Wilkinson power combiner to novel modified Wilkinson power combiner.

Table 17: Wilkinson power combiner parameters.

Parameter	Values
Frequency (GHz)	9.5
Dielectric constant, ε_r	2.95
Dissipation factor (Tan δ)	0.0025
Substrate thickness (mil)	2
Conductor thickness (μm)	9
Electrical length (º)	90
35.4 Ω line[+] width (μm) / Length (μm)	205 / 4801
50 Ω line[+] width (μm) / Length (μm)	120 / 4916
70.7 Ω line[+] width (μm) / Length (μm)	64 / 5054

[+] Microstrip

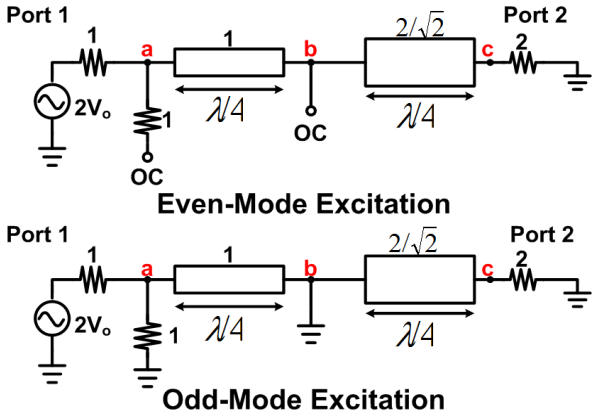


Figure 106: Even-mode and odd-mode excitations of the modified Wilkinson power combiner.

For the even-mode excitation, looking into Port 1, the even-mode impedance at point *a* can be expressed as

$$Z_a^e = \frac{\left(2/\sqrt{2}\right)^2}{2} = 1. \tag{77}$$

Using the voltage divider rule, the voltage drop for the even-mode excitation is expressed at point *a* as

$$V_a^e = \frac{2V_0}{1+1} = V_o \ , \tag{78}$$

and at point *b* as

$$V_b^e = -jV_o \, . \tag{79}$$

The voltage on a transmission line is expressed as a sum of the incident and reflected waves as follows:

$$V(x) = V^+(e^{-j\beta x} + \Gamma e^{j\beta x}), \tag{80}$$

where $e^{-j\beta x}$ represents the incident wave propagating in the $+x$ direction, $e^{j\beta x}$ represents the reflected wave propagating in the $-x$ direction, V^+ is the voltage constant determine by the boundary conditions, β is the phase constant, and Γ is the reflection coefficient. By

letting $x = -\lambda/4$ at point *b* and x = 0 at point *c*, through (80), the voltage drop for the even-mode excitation is expressed at point *b* as

$$V_b^e = V(-\lambda/4) = jV^+(1-\Gamma) = -jV_o, \tag{81}$$

and at point *c* as,

$$V_c^e = V(0) = V^+(1+\Gamma) = -V_o\frac{1+\Gamma}{1-\Gamma}. \tag{82}$$

The reflection coefficient at point *c* is expressed as

$$\Gamma = \frac{2-2/\sqrt{2}}{2+2/\sqrt{2}}, \tag{83}$$

and through (82) to (83), the voltage drop for the even-mode excitation at point C is expressed as

$$V_c^e = -V_0\sqrt{2}. \tag{84}$$

For the odd-mode excitation, by looking in the Port 1, the odd-mode excitation at point a is expressed as

$$Z_a^o = 1, \tag{85}$$

since the short circuit at point *b* appears like an open circuit at point *a*, because of the quarter-wave transformer. The voltage drop for the odd-mode excitation is expressed at point *a* as

$$V_a^o = \frac{2V_0}{1+1} = V_o \tag{86}$$

and at points *b* and *c* as

$$V_b^o = V_c^o = 0. \tag{87}$$

Figure 107 shows the impedances at various points in the modified Wilkinson power combiner. When the impedances at the three ports are matched to 50 Ω, the normalized impedances at points *a*, *b*, and *c* are expressed as

$$Z_{in\_port1} = Z_{in\_port3} = Z_{in\_port2} = 1. \tag{88}$$

A quarter-wave transformer with normalized impedance of $\frac{1}{\sqrt{2}}$ is added between point *b* and *c*, so that the internal impedances at point *b* are matched equally, where

$$Z_{in\_T1} = Z_{in\_T2} = (1/\sqrt{2})^2 = 1/2 \ . \tag{89}$$

Through (88) to (89),

$$S_{11} = S_{22} = S_{33} = 0, \tag{90}$$

as the ports are all externally matched to 50 Ω. It is assumed that there is no current flow between points *a* and *d*, since they share the same potential difference,

$$S_{13} = S_{31} = 0. \tag{91}$$

Combining the even-mode and odd-mode excitations, the voltage transfer between Port 2 and Port1/Port3 can be shown as

$$S_{21} = S_{12} = S_{32} = S_{23} = \frac{V_c^e + V_c^o}{V_a^e + V_a^o} = \frac{-V_o\sqrt{2}}{V_0} = -\frac{1}{\sqrt{2}} . \tag{92}$$

Through (90) to (92), the S-parameter matrix for the novel modified Wilkinson power combiner is expressed as

$$-\frac{1}{\sqrt{2}}\begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix}. \tag{93}$$

From (93), it is shown that the modified Wilkinson power combiner is a 3-dB and 180° phase power combiner.

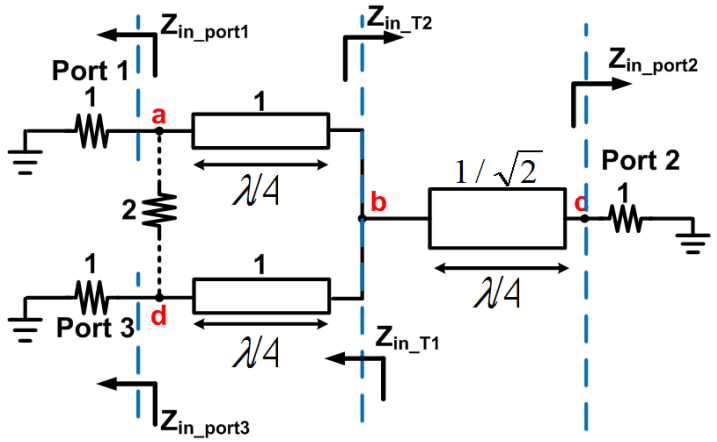


Figure 107: Impedances in the modified Wilkinson power combiner.

The modified Wilkinson power combiner is designed at 9.5 GHz. The size of the power combiner is about 9.4 x 3.9 mm^2, as shown in Figure 108. The surface-mounted 100 Ω resistor has a dimension of 1.0 by 0.5 mm^2 and a thickness of 0.4 mm. The EM simulated and measured S-parameters are shown in Figure 109. At 9.5 GHz, the measured insertion loss of the power combiner is about 0.4 dB, S_{11} is about -13.5 dB, S_{22} is about -18 dB, and the isolation between Port 1 and Port 3 is about 26 dB.

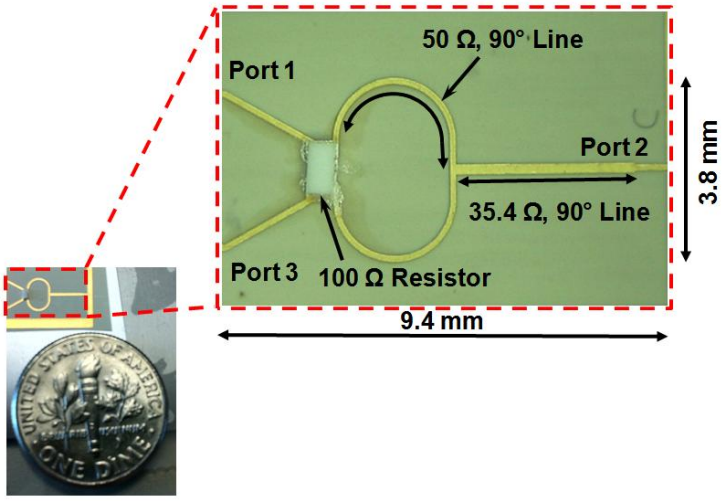


Figure 108: Modified Wilkinson power combiner.

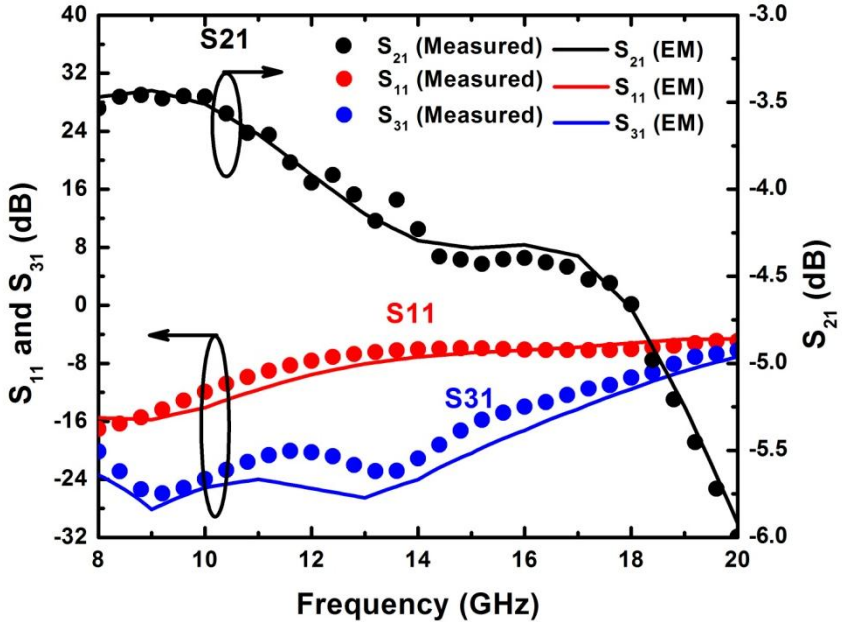


Figure 109: Simulated and measured S-parameters of the modified Wilkinson power combiner.

8.5.3 Package

Figure 110 shows the wirebonded package for two SiGe LNAs. The package is divided into three stages, namely the input stage, the LNA stage, and the output stage. The input stage consists of two 50 Ω microstrip lines. Each microstrip line has a length of 4528 μm. In the LNA stage, there are two SiGe LNAs epoxy-attached on the LCP. The LNA pads are connected to LCP CPW lines through the wirebonds. At the output stage, LNA signals are combined through the Wilkinson power combiner.

The embedded flip-chip package has a similar layout as the wirebonded package, except the wirebond interconnects are replaced by the Au bumps and the LCP vias. The SiGe LNAs are embedded underneath the LCP, as shown in Figure 111. In the embedded flip-chip package, two SiGe die are placed side by side and the spacing between them is kept at least 280 μm, as shown in Figure 112.

For both the packages, Port 1 and Port 3 were measured using a dual GSG probe (GGB model 40A-GSG-150 / 40A-SG-150-D-300) and Port 2 was measured using a GSG probe (GGB model 40A). All measurements were performed on the top side of the LCP substrates. The VNA was calibrated based on a SOLT standard using a CS-2-150 calibration substrate.

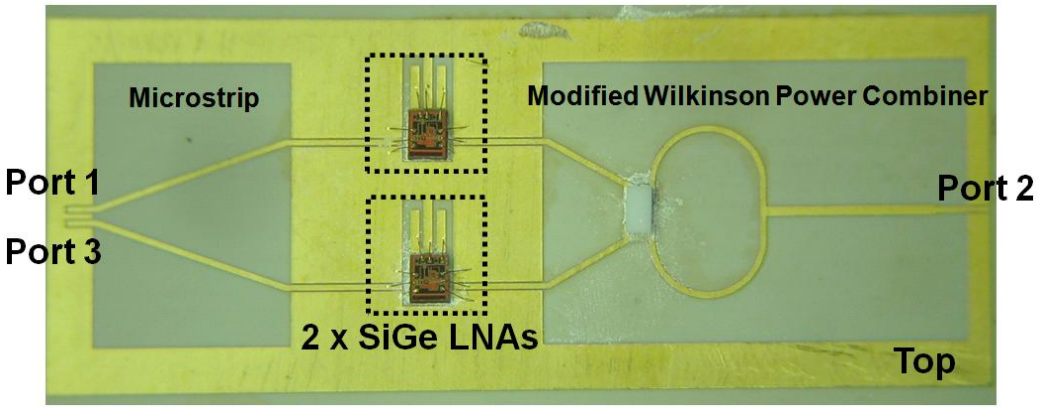
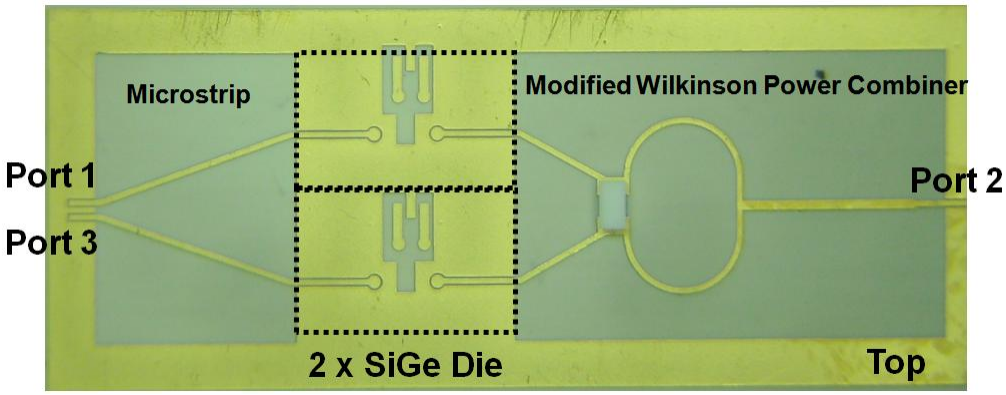
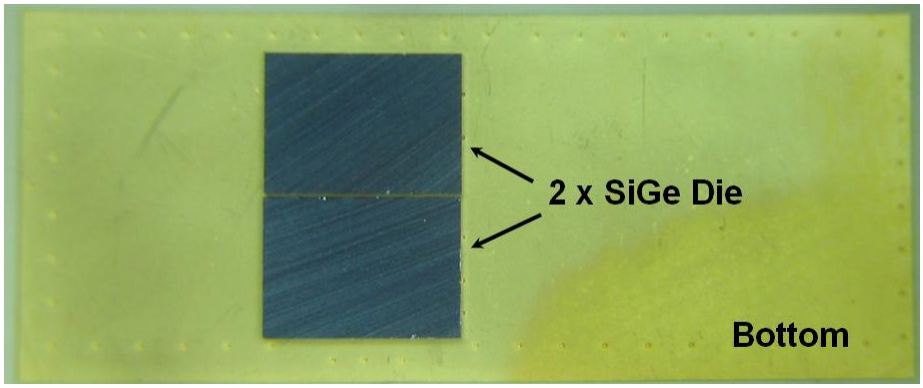


Figure 110: Wirebonded package for two SiGe LNAs.



(a)



(b)

Figure 111: Embedded flip-chip package for two SiGe LNAs: (a) top view and (b) bottom view (without the LCP lid).

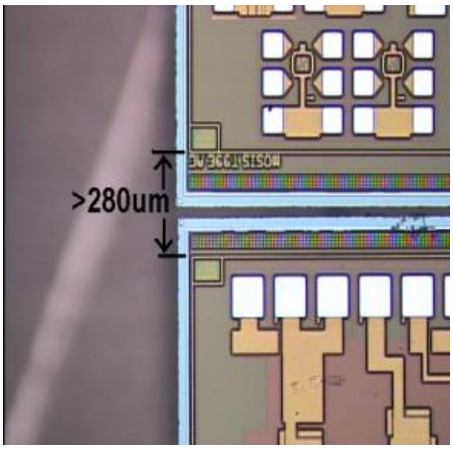


Figure 112: Minimum spacing between two SiGe LNA die for the embedded flip-chip package.

Figure 113 shows the measured results for the wirebonded and embedded flip-chip packages. The ideal S-parameter results are based on lossless interconnects and the S_{21} is 17.2 dB at 9.5 GHz. For the wirebonded package, the measured S_{21} is about 14.2 dB, while the embedded flip-chip package is about 16.5 dB. The wirebonded package shows larger degradation in the S_{11} and S_{22} results. The worst case return loss for the wirebonded package is about 9.9 dB, while the flip-chip package is about 16.3 dB. Overall, the flip-chip package has measured S-parameters that are closer to the ideal S-parameters.

As shown in Figure 113, when more circuits are integrated together, there is a tendency to induce more degradation and performance uncertainties to the system, because of the increasing mismatch elements in the package. Thus, it is important to model the package interconnects, so that the package-induced parasitics are taken into consideration during the design phase and any losses due to the interconnects can be compensated.

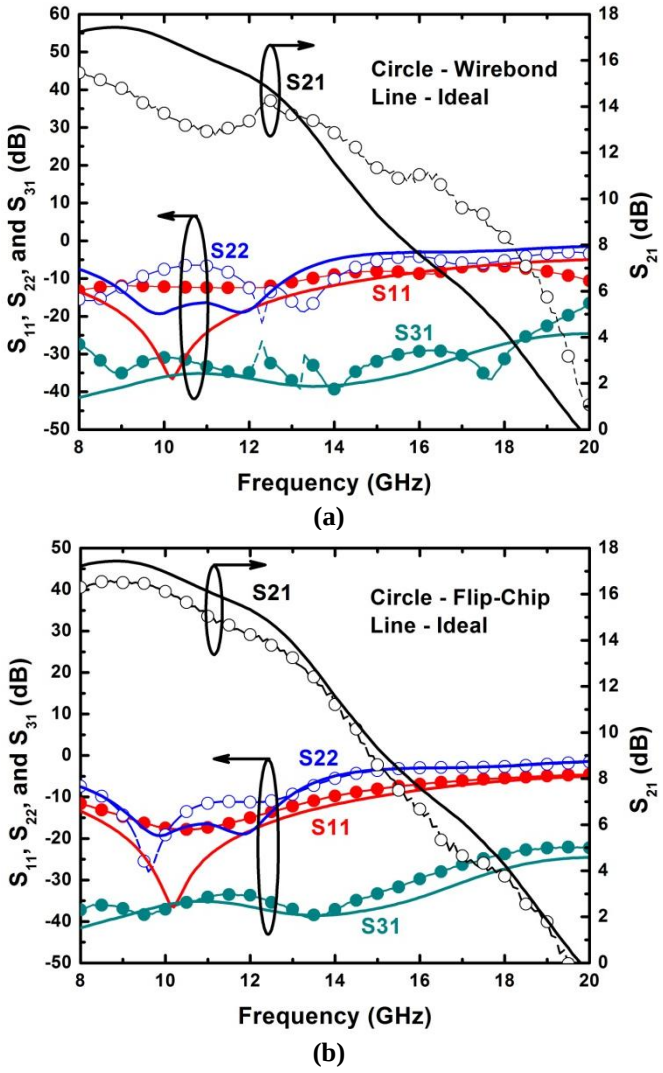


Figure 113: Measured S-parameter results of the two SiGe LNAs packages: (a) magnitude of the wirebonded package in dB and (b) magnitude of the embedded flip-chip package in dB.

8.5.4 Modeling

Full-wave EM simulations were performed for the wirebond and embedded flip-chip interconnects using Ansoft HFSS 3-D EM software, from 8 to 20 GHz. The wirebond interconnect consists of wires that connect between the LNA pads and the LCP CPW line, while the flip-chip interconnect consists of Au bumps and the LCP via, as

shown in Figure 114. For the EM-simulated structures, the package interconnects are cascaded with LCP CPW lines.

S-parameter matrices of the EM-simulated structures are first converted into their equivalent ABCD transmission matrices. The ABCD matrices of the CPW lines are then measured and the test structures are de-embedded through (94).

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Interconnect} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{CPW}^{-1} \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Test\_Structure} . \quad (94)$$

From (20), the interconnect ABCD matrix of a package interconnect is translated into a 2-port π equivalent circuit, as shown in Figure 115. The lumped elements in the π equivalent circuit are derived through (95) to (98).

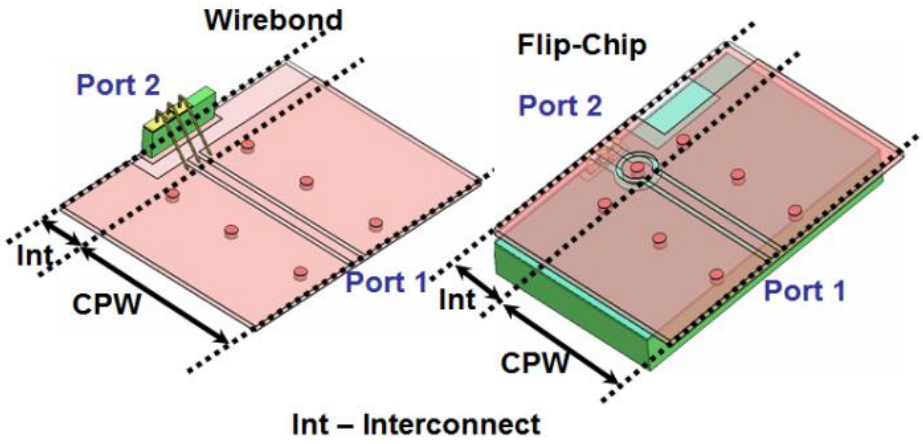


Figure 114: EM-simulated structures for the package interconnects.

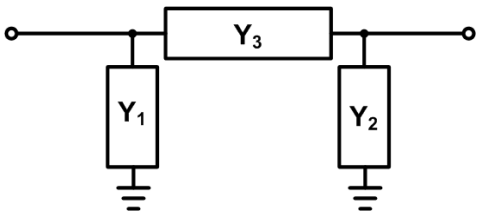


Figure 115: Lumped-element π equivalent circuit.

$$A = 1 + \frac{Y_2}{Y_3}, \tag{95}$$

$$B = \frac{1}{Y_3}, \tag{96}$$

$$C = Y_1 + Y_2 + \frac{Y_1 Y_2}{Y_3}, \tag{97}$$

and

$$D = 1 + \frac{Y_1}{Y_3}. \tag{98}$$

Agilent Advanced Design System (ADS) was used to further optimize the lumped elements to correlate the EM simulated results with the model simulated results. Figure 116 shows the models for the wirebond and embedded flip-chip interconnects. In both models, the Y_1 and Y_2 are mainly capacitive. Y_1 denotes the discontinuity at the LCP CPW line, while Y_2 denotes the discontinuity at the SiGe pad. Y_3 is mainly resistive and inductive, because of the skin effect and ohmic loss present in the interconnect.

From the models shown in Figure 116, the embedded flip-chip package induces less parasitics compared to the wirebonded package. The interconnects for the flip-chip package are shorter in the length and are thicker in diameter. Moreover, the wirebond interconnect model has an additional capacitor that is connected in parallel with the resistor and inductor in Y_3. To relieve the tension in the wire ball-bond, a wire loop is usually formed during the bonding process which could create the extra capacitance.

The EM-simulated and model-simulated S-parameter results are shown in Figure 117. The model-simulated results match closely with the EM-simulated results, from 8 to 20 GHz.

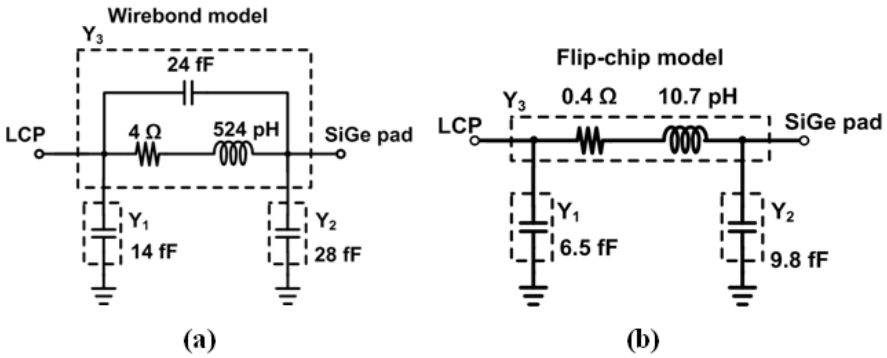


Figure 116: Interconnect models: (a) wirebond interconnect and (b) embedded flip-chip interconnect.

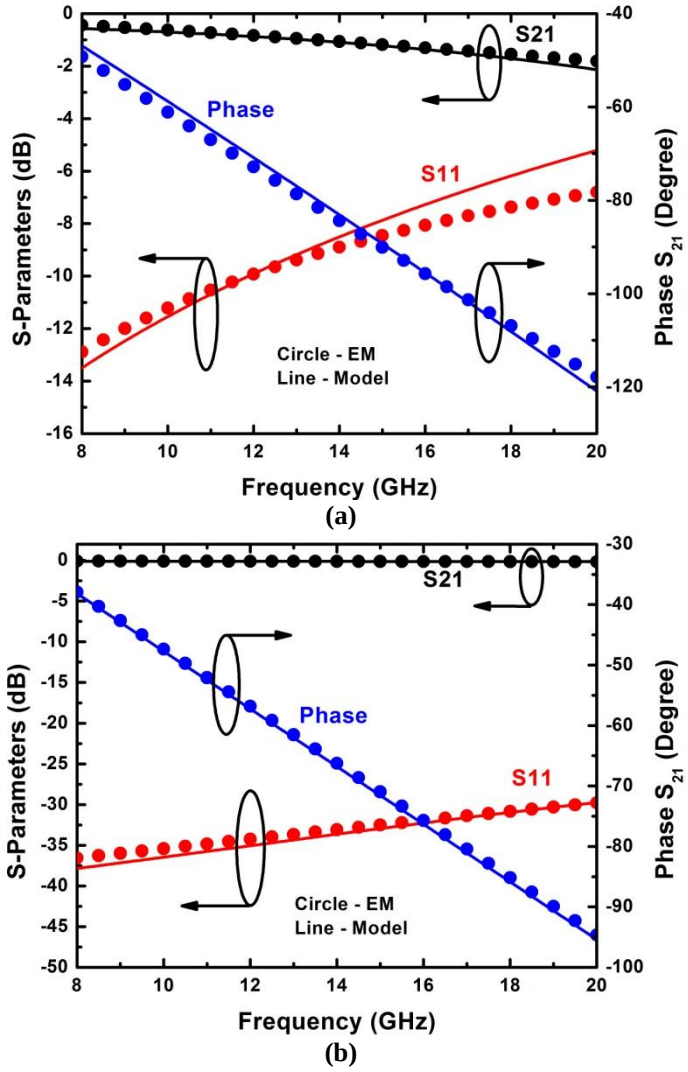


Figure 117: S-parameter results and phase response: (a) wirebond interconnect and (b) embedded flip-chip interconnect.

Figure 118 shows the measured and modeled S-parameter results for the single SiGe LNA packages. Figure 119 shows the measured and modeled S-parameters results for the two SiGe LNAs packages. As shown in Figures 118 and 119, the model simulations show reasonably good match with the measured results. For the wirebond interconnects, there is a slight discrepancy between the model simulations and measured results, because of the variations in the wire lengths. Moreover, the model extractions of the interconnections are based on their EM simulated results. Hence, it is expected to see slightly differences between the measured and the model-simulated results. Nevertheless, the model simulations help to predict the circuit performances, so that optimization can be done accordingly and minimize any uncertainties in system.

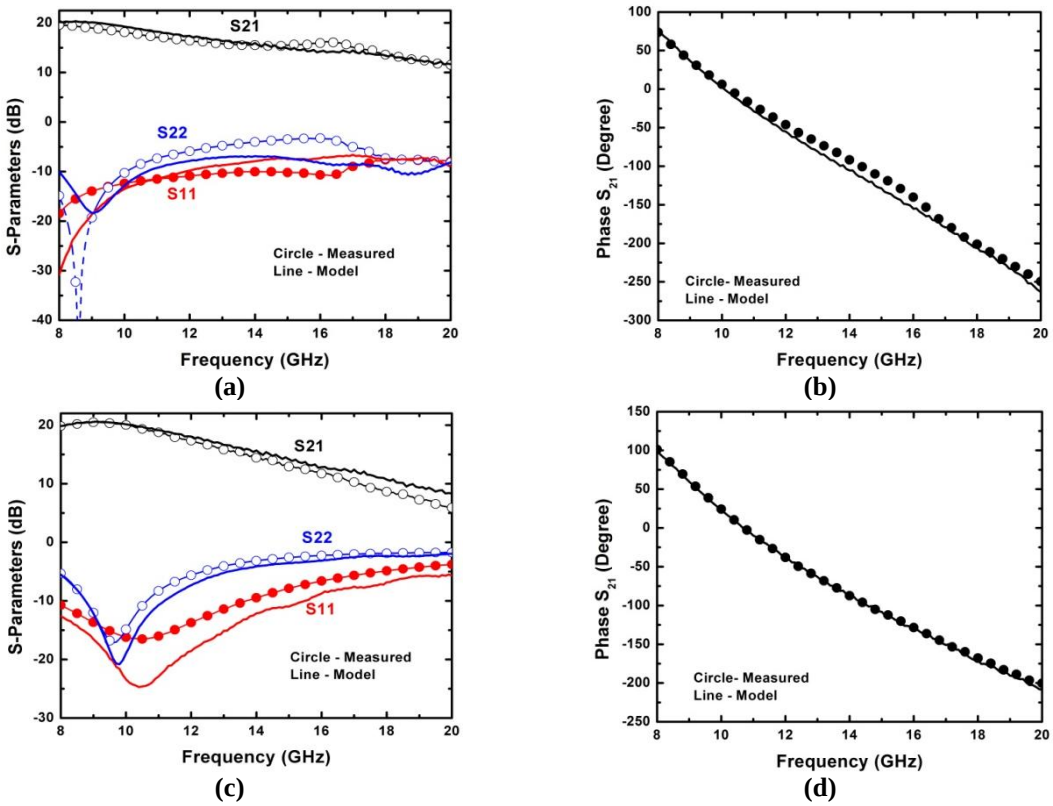


Figure 118: Model and measured S-parameter results of the single SiGe LNA packages: (a) magnitude of the wirebonded package in dB, (b) phase response of the wirebonded package in degree, (c) magnitude of the embedded flip-chip package in dB, and (d) phase response of the embedded flip-chip package in degree.

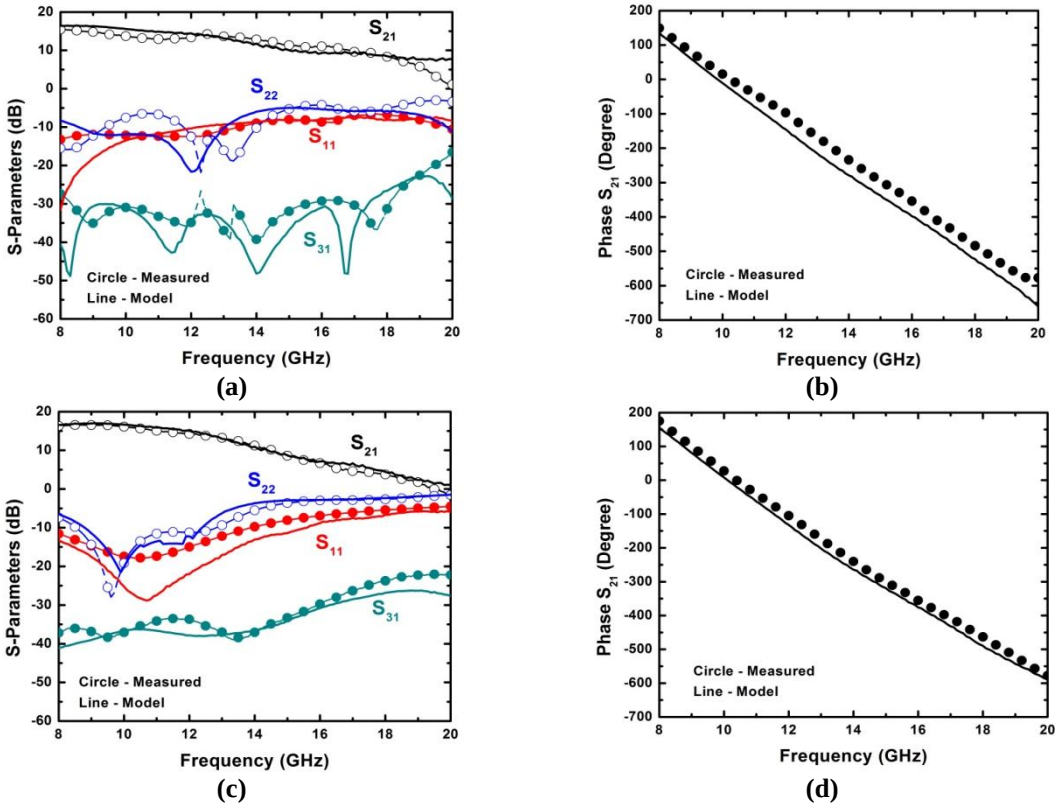


Figure 119: Model and measured S-parameter results of the two SiGe LNAs packages: (a) magnitude of the wirebonded package in dB, (b) phase response of the wirebonded package in degree, (c) magnitude of the embedded flip-chip package in dB, and (d) phase response of the embedded flip-chip package in degree.

Also through the modeling process, we see an improvement in the matching between the measured and the simulated results, as compared using just the ideal simulation result to predict the system behavior. Therefore, incorporating the interconnect models in the circuit designs helps to improve simulation accuracies and at the same time, reduces the complexity and time in running full-wave EM simulations for the whole packages. Figure 120 shows four LNAs combined through the modified Wilkinson power combiners. In this case, the model simulation is used to replace the EM simulation, since there are more package interconnects and it is going to take a much longer time for the EM software to compute the S-parameters. As shown in Figure 121, the S-parameters can be predicted much faster with the model simulation. At 9.5 GHz, it is shown that the flip-chip package has a lower insertion loss and a better impedance match than the

wirebonded package. Thus, the model simulation can be implemented in a larger system to reduce the simulation time.

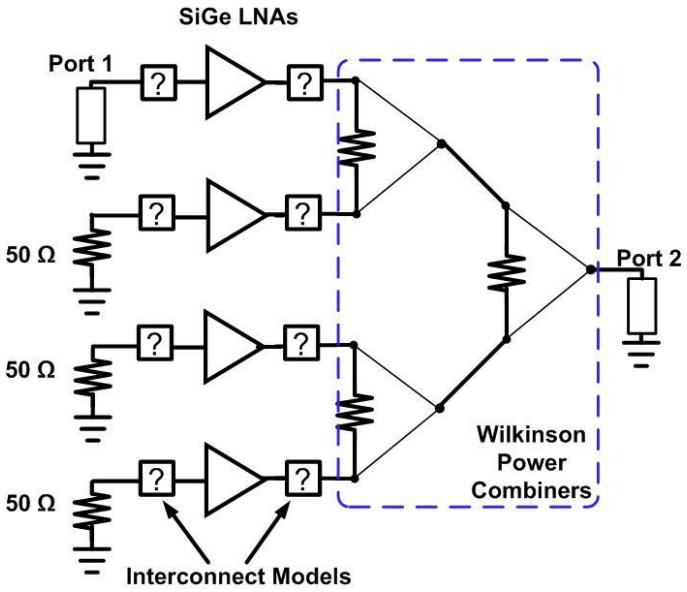


Figure 120: Schematic of four LNAs combined together with the interconnect models.

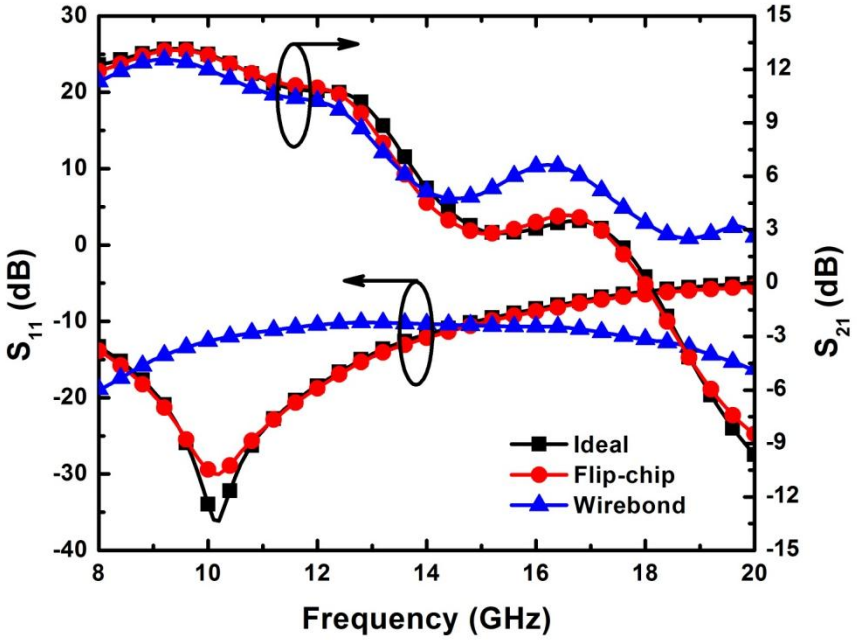


Figure 121: Model simulations of four LNAs combining together with the interconnect models.

8.6 Summary

This dissertation presents the comparisons of wirebonded and embedded flip-chip packages using X-band SiGe LNAs. For the first time, multiple die are put together in a single package to compare the packaging effects and to demonstrate the feasibility of embedding multiple dies within a single package. At high frequencies, the wirebond interconnect introduce more parasitics than the flip-chip interconnect, which degrades the system performances. The embedded flip-chip packages have shown very promising results and they are close to the ideal S-parameter results. Tables 18 and 19 show the S-parameters comparisons of X-band SiGe LNAs with different packages. At X-band, the embedded flip-chip packages show superior performances over the wirebonded packages. A novel approach to design a modified Wilkinson power combiner to overcome fabrication limitations is proposed. The modified Wilkinson power combiner has insertion loss of less than 0.4 dB and isolation of 26 dB at 9.5 GHz. Equivalent circuit models for the wirebond and embedded flip-chip interconnects have been extracted and validated with the measured data from 8 to 20 GHz. The model simulations are very useful especially in applications, where there are too many interconnects in the system and the EM simulations can be extremely complicated or nearly impossible to run.

Table 18: S-parameters comparison between packages for single SiGe LNA.

	Frequency (GHz)	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)
1 x SiGe LNA (ideal)	9.5	20.7	-20.9	-19.3
1 x SiGe LNA (embedded flip-chip package)	9.5	**20.3**	**-15.1**	**-16.8**
1 x SiGe LNA (wirebonded package)	9.5	18.5	-13.0	-13.2

Table 19: S-parameters comparison between packages for two SiGe LNAs.

	Frequency (GHz)	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)	S_{31} (dB)
2 x SiGe LNAs (ideal)	9.5	17.2	-21.5	-22	-37.6
2 x SiGe LNAs (embedded flip-chip package)	9.5	**16.5**	**-16.3**	**-25.5**	**-38.3**
2 x SiGe LNAs (wirebonded package)	9.5	14.2	-12	-9.9	-32.8

CHAPTER IX

CONCLUSION AND FUTURE WORK

9.1 Summary of Contributions

This dissertation focuses on developing T/R modules using SiGe HBT BiCMOS technology with LCP package for the next-generation phased-array radar system. The developed RF circuit blocks include a PA, a tunable filter, an LNA, and a SPDT switch, operating at X-band. In addition, the package interconnect issues are discussed in this dissertation. The contributions of this research are as follows:

1. Design of an X-band SiGe PA for radar front-ends. The PA used a cascode architecture to increase its breakdown voltage. The PA has a gain of 15.4 dB , an output P_{1dB} of 16 dBm, an output P_{sat} of 19 dBm, and maximum PAE is 18.5% Considering the size, the gain, and the P_{out}, the PA presented in this dissertation has the highest FOM as compared to other X-band SiGe PAs.
2. Design of a monolithic X-band tunable filter. The filter consists of two stages: the gain stage and the filter stage. The integration capabilities offered by the SiGe HBT BiCMOS technology enable a SiGe filter to integrate with a SiGe HBT LNA, which improves the insertion loss and the noise figure. The X-band tunable filter presented in this dissertation consumes a minimal *dc* power (P_{dc}) of 2.75 mW, has an insertion loss of less than 1.2 dB, a low NF of less than 3.8 dB, and a wide tuning range, as compared to other active filters. The tunable filter can be used to replace the switched filter banks in multiband receivers, so that number of filters used, the cost, and the size of the system can be reduced drastically.
3. S-parameter measurements of an X-band tunable filter across temperatures (90 to 398 K). At cryogenic temperature (90 K), the filter bandpass gain shows an improvement of more than 1 dB. At high temperature (398 K), the degradation in the bandpass gain is less than 2.7 dB. Across the temperatures, the shift in the f_c is

less than 0.8 GHz. This demonstrates the potential of operating a SiGe filter in extreme environments.

4. A new methodology to extract parasitics for via interconnect models. The approach of using a single via structure with embedded capacitors to extract the via parasitics is straightforward, as the EM simulation for a single via takes shorter time to run and minimal effort is required to design the embedded capacitors which can be fabricated using standard PCB process.
5. A new methodology to de-embed pad parasitics from test structures at high frequencies. EM software was used to model the pads since the EM software is able to capture most of the needed EM phenomena. Based on the EM simulation results, the pads were directly de-embedded from the test structures. As compared to other conventional de-embedding methods, the EM-simulated-pad de-embedding method proves to be most accurate and shows good agreement up to 67 GHz.
6. Design and analysis of a low-power and low-voltage SiGe HBT LNA. The LNA was designed using a common-emitter configuration and operating at different biasing modes: forward-active (FA) and weak-saturation (WS). For the same amount of power consumption at 1 mW, the SiGe LNA has a higher gain when biasing in the WS mode as compared to the FA mode. In WS mode, when the collector voltage (V_{cc}) and collector current (I_c) are set at 0.5 V and 1 mA, respectively, the SiGe LNA achieves a gain of more than 8.5 dB at 10 GHz. This yields a gain per *dc* power consumption FOM of 17 dB/mW. This is by far the highest reported to date for X-band SiGe LNAs.
7. Comparison between the different types of on-chip transmission lines: microstrip (MS) and conductor-backed coplanar waveguide (CPW). Generally, CPW lines have better RF performances than MS lines, because of the additional ground shielding. However, for compact design and layout simplicity, MS lines are

preferred, since at X-band, both MS and CPW lines have the similar RF performances.

8. Design of an X-band to Ka-band SPDT switch. The proposed SiGe SPDT switch used diode-connected SiGe HBTs that have very broadband characteristics. The design utilized a series-shunt configuration, which further improves the isolation. Between 8 and 40 GHz, this SiGe SPDT switch has an insertion loss of less than 4.3 dB and an isolation of more than 20.3 dB, and consumes only 5.6 mW of power. The proposed SiGe SPDT switch has the broadest operating bandwidth of any SiGe SPDT switch that has been reported to date.
9. Investigation of packaging effects of X-band SiGe LNAs embedded in an organic LCP substrate. Two different RF packaging approaches were compared: the wirebonded and the embedded flip-chip packages. At X-band, the embedded flip-chip packages have better RF performances than the wirebonded packages.
10. Demonstration of embedding multiple SiGe die in multilayer LCP substrates leading towards the development of 3-D SOP architectures for compact low-cost wireless front-end systems.
11. Design of a novel modified Wilkinson power combiner. The modified Wilkinson power combiner is a 3-dB and 180° phase power combiner. Fabricating a standard Wilkinson power combiner on a thin substrate can be challenging as the line width gets narrow. The proposed modified Wilkinson power combiner helps to overcome this concern and ease the fabrication process, making the design more realizable
12. Modeling the package interconnects between the SiGe MMICs and the LCP package, so that the time and complexity of running the EM simulations can be reduced drastically. This is very useful in situations where there are many MMICs in a single package, which involves many interconnects.

9.2 Future Work

This dissertation work has covered the RF performances of individual circuit blocks in a T/R module at X-band. Further work is needed to improve the performance and reliability of the T/R module. In the future, this research work can be extended by:

1. Designing a high-power 1 W SiGe PA at X-band. At present, most high-power PAs are designed using III-V technologies. Although the peak f_T of the SiGe HBTs has increased dramatically over the years, their breakdown voltages are still much lower than the III-V technologies, which limit the PA P_{out}. Power combiners can be used to boast the P_{out} but at the same time, decreasing the PA gain because of more interconnects are being introduced. It is important that these interconnects are well-modeled so that the PA can be optimized accordingly to minimize the insertion loss.
2. Investigating the PA performance at cryogenic temperatures. At present, most cryogenic RF measurements are done based on SiGe LNAs. It is well-known fact that the SiGe LNA has a higher current gain at lower temperature. However, very few studies are done on SiGe PA at cryogenic temperatures and thus the PA linearity performance at cryogenic temperatures remains unclear.
3. At present, the silicon switches have a lower power handling than the III-V switches. New topology for silicon switches have to be implemented to improve the power handling capability. Alternatively, the number of T/R modules in a system can be increased, so that the PA P_{out} can be lowered and the silicon switch is able to handle.
4. Investigating the reliability of the LCP packages across temperatures. So far, most of the RF measurements for the LCP packages are performed at room temperature. It will be interesting to observe how the LCP packages respond at different temperature cycles, so that the potential use of the LCP packages for extreme environment applications can be evaluated.

5. Developing the SiGe T/R modules for millimeter-wave applications. The f_t and f_{max} of SiGe HBT technology have improved dramatically over the years.
6. Understanding the thermal issues in T/R module packaging. High-power PAs in the T/R modules tend to generate large amount of heat during operation. Various methods of cooling down the PAs have to be investigated, so that the PA efficiency can be improved and more high-power PAs can then be integrated into the T/R modules.

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VITA

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